

Replacing Crystals and Oscillators

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One PhaseLink IC can replace multiple crystals or oscillator modules. However, some care has to be taken about connecting the PhaseLink IC output to the target crystal pin or CMOS input. This application note will describe the following connections:

- 1) Replacing a crystal: How to connect the PhaseLink IC output to a crystal pin.
- 2) Replacing an oscillator module: How to connect the PhaseLink IC output to a CMOS input with the following conditions:
 - a) $VDD1 = VDD2^*$
 - b) $VDD1 > VDD2$
 - c) $VDD1 < VDD2$

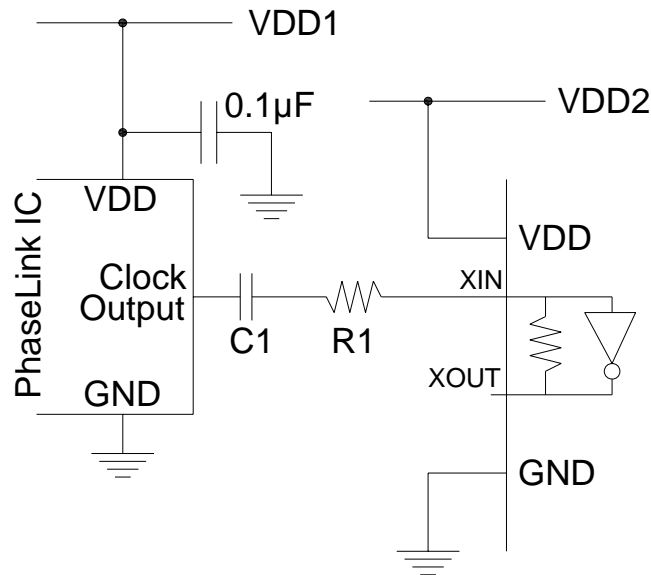
* $VDD1$ is the supply voltage of the PhaseLink IC and $VDD2$ is the supply voltage of the circuit with the target input.

1) Replacing a Crystal

PhaseLink IC's often replace a number of crystals in the application. This means that a Clock Output needs to drive a pin of the crystal oscillator. I would like to make the following suggestions for driving a crystal pin:

- 1) Use the XIN pin or "crystal oscillator input" pin to drive the clock signal into.
- 2) Use AC coupling from Clock Output to the crystal oscillator pin. This allows the biasing of the crystal oscillator to do its job. However if the signal amplitude from the Clock Output is large enough, C1 may not be necessary.
- 3) Select a low VDD value for the PhaseLink IC, if possible. When using AC coupling it is not necessary to have a large amplitude from the Clock Output. Depending on the crystal oscillator circuit, it may be better to have a lower amplitude to make the signal more similar to a crystal signal. The biggest advantage may be a very low power consumption of the PhaseLink IC at a low voltage (e.g. 1.8V).
- 4) Use low drive strength for the Clock Output buffer. When using a crystal the waveform will be a sine wave. Low drive strength would slow down rising and falling edges of the signal and making it look as much as possible like a sine wave. The drive strength can be further reduced with a series resistor (see R1 in the circuit on the next page).

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(Diagram 1)

The value of C1 is difficult to determine in this document, not knowing any details about the XIN pin. As mentioned above, we can take the easy way out and select a large value like 1000pF or larger.

Sometimes a more square wave looking signal with a large amplitude on XIN causes more cross-talk of this signal to other circuitry. Using a series resistor R1 can solve the issue. The best value for R1 depends upon the frequency and the XIN input capacitance (C_{XIN}). This capacitance can be quite large, like 20pF or 30pF. The best value for R1 can be calculated as follows: $R1 = 1 / (2\pi \times F \times C_{XIN})$

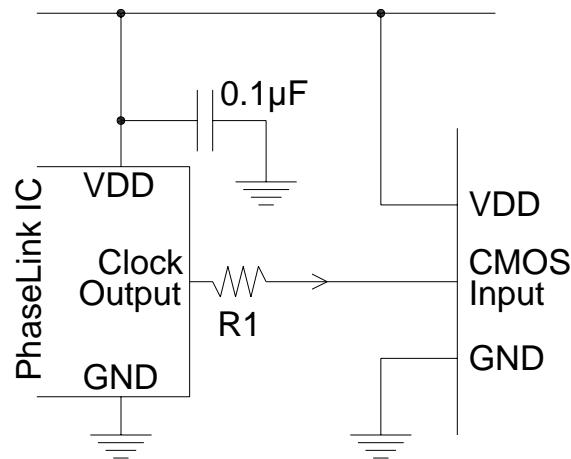
Example: $F = 20\text{MHz}$ and $C = 30\text{pF}$

$$R1 = 1 / (2\pi \times 20\text{MHz} \times 30\text{pF}) = 265\Omega$$

The closest commercially available value would be 270Ω.

2a) Replacing an oscillator

When driving a CMOS input from a clock output on a PhaseLink IC, the general advice is to use the same VDD voltage on both the PhaseLink IC and the IC that is receiving the signal. You can make a direct connection without the need of additional components. When the distance between the Clock Output and the CMOS Input is large so you see reflections on the signal at the CMOS Input, you can use R1 to match the Clock Output impedance to the trace impedance. The output impedance of the Clock Output usually is near 20Ω and when the trace is designed for a 50Ω impedance, you would need $R1 = 30\Omega$.



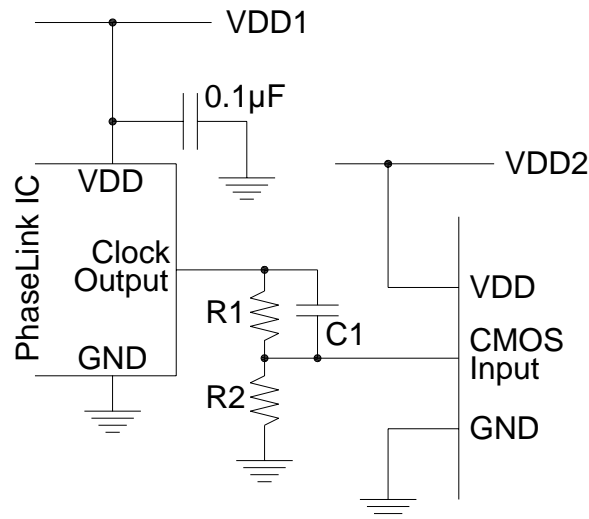
(Diagram 2)

This is the simplest application and probably the most used also. However there are situations where the VDD on the PhaseLink IC and the circuit with the CMOS input is different. The following pages will address a number of different situations and suggest circuits to deal with those situations.

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2b) Replacing an oscillator

When driving a CMOS input on a chip with a lower supply voltage, the clock signal needs to be attenuated. This can be done with two resistors and a capacitor:



(Diagram 3)

In this case VDD2 is smaller than VDD1. The resistor divider attenuates the amplitude and C1 corrects the rise/fall time speed. C1 may not be necessary depending on rise/fall time requirements.

Configuring R1, R2 and C1:

R1 and R2 will cause some extra supply current. The current can be calculated with the following formula: $I_{Network} = VDD1 / (2 \times (R1 + R2))$. Lets say that we want $I_{Network}$ to be 0.1mA with VDD1=3.3V, then $R1 + R2 = 16500\Omega$.

Next we can calculate R2: $R2 = (R1 + R2) \times VDD2 / VDD1$.

Finally we can calculate R1: $R1 = (R1 + R2) - R2$.

Example: VDD1=3.3V, VDD2=1.8V and $I_{Network} = 0.1mA$

$$(R1 + R2) = 3.3 / (2 \times 0.1mA) = 16500\Omega.$$

$$R2 = 16500 \times 1.8 / 3.3 = 9000\Omega.$$

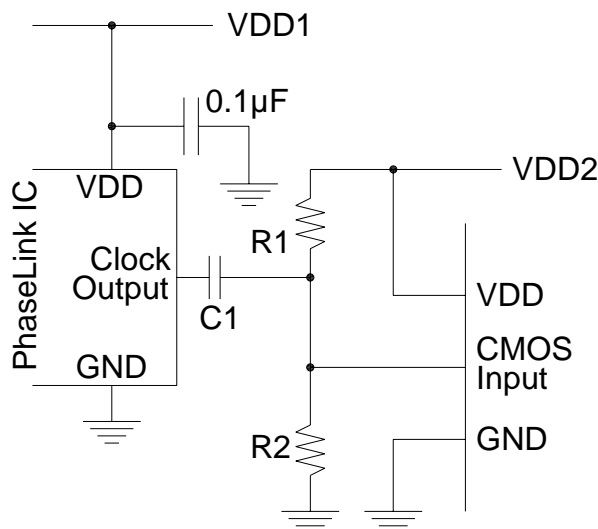
$$R1 = 16500 - 9000 = 7500\Omega.$$

Without C1 the rise/fall times will be at least $C_{Input} \times R1 \times R2 / (R1 + R2)$ where C_{Input} is the input capacitance of the CMOS input. Lets assume C_{Input} is 3pF with above network, the rise/fall will be at least $3pF \times 9000 \times 7500 / (9000 + 7500) = 12.3ns$. If this is too slow, the rise/fall times can be corrected with C1. The formula is: $C1 = C_{Input} \times R2 / R1$. In case of the example, $C1 = 3pF \times 9000 / 7500 = 3.6pF$.

The ratio between R1 and R2 is more important than the absolute values of R1 and R2. When we use $R1 = 10000\Omega$ and $R2 = 12000\Omega$, we have the same ratio but with easy commercially available values. The current through the network is now 0.075mA, all other properties will remain the same.

2c) Replacing an oscillator

When VDD on the PhaseLink IC is lower than VDD on the circuit with the CMOS input, we need to use a different network.



In this case VDD1 is smaller than VDD2. This network with R1, R2 and C1 will shift the average level of the Clock Output signal to the threshold point of the CMOS Input. For most CMOS inputs this $V_{\text{Threshold}}$ is 50% of VDD which makes $R1 = R2$. In this case also the network draws a little bit of current. The current will be $VDD2/(R1+R2)$.

With 0.1mA and $VDD2=3.3V$, $R1+R2 = 33000\Omega$ and $R1 = R2 = 16500\Omega$. For commercially available values we can use 18000Ω or 22000Ω , where the network current reduces to resp. 0.092mA and 0.075mA.

When $V_{\text{Threshold}}$ is not 50%VDD then we can calculate R1 and R2 as follows:

$$R2 = (R1+R2) \times V_{\text{Threshold}} / VDD2$$

$$R1 = (R1+R2) - R2.$$

C1 simply needs to be large enough to not cause any significant attenuation. The -3dB point of the high-pass network with C1, R1 and R2 is:

$$F_{-3dB} = (R1+R2) / (2\pi \times R1 \times R2 \times C1) \text{ or } C1 = (R1+R2) / (2\pi \times F_{-3dB} \times R1 \times R2)$$

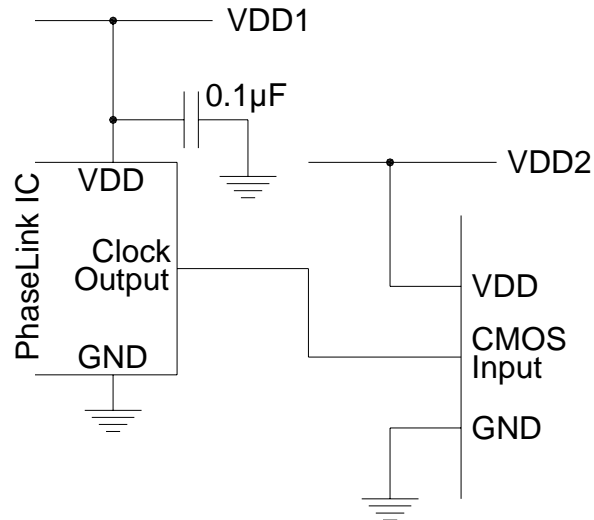
Lets say the lowest Clock Output frequency is 10MHz and we want F_{-3dB} to be at least 10x below this point at 1MHz maximum.

With $R1 = R2 = 22000$: $C1 > (22000+22000) / (2\pi \times 1000000 \times 22000 \times 22000) = 14.5pF$. So $C1=15pF$ or larger should be OK. The easy way out is to select $C1 = 1000pF$ or larger to be able to pass almost any signal.

There is one issue with this method: The signal on the CMOS Input will not swing rail-to-rail on this input. The amplitude is set by VDD1. For example when $VDD1 = 1.8V$, then the signal amplitude is 1.8Vpp. When $VDD2 = 3.3V$, then the signal on the CMOS Input will swing between 0.75V (=23%VDD) and 2.55V (=77%VDD). It depends upon the CMOS Input level requirements if this is OK or not. Usually CMOS inputs are fine with 40% / 60% level and certainly with 30% / 70% levels.

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When VDD1 and VDD2 are close, you may consider not using the network and simply connect straight from Clock Output to CMOS Input.



For example with VDD1=2.5V and VDD2=3.3V, the signal high level on the CMOS Input is 2.5V or 76% of VDD2. It still complies with a 30% / 70% signal level requirement. So without the network you will have signal levels of 0% / 76% and with the network with R1, R2 and C1 the levels would improve to 12% / 88%.