PhaseLink Application Note

Programmable versus non-programmable clocks

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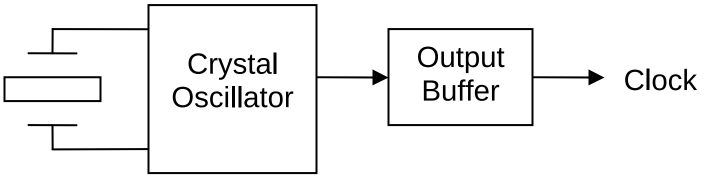
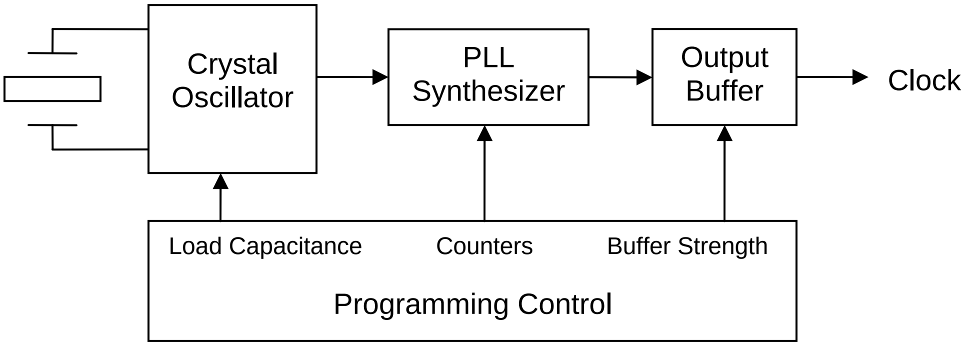
When PhaseLink is presenting their PL611s programmable clock oscillator to oscillator manufacturers, the PL611s is often compared with the older technology non-programmable clock oscillator chips. However, the programmable PL611s is much more complex inside and has certain behavior that sometimes confuses users. See below simple block diagrams, comparing the programmable PL611s with the non-programmable plain crystal oscillator.

Non-programmable plain crystal oscillator:



PL611s programmable crystal oscillator:



(Diagram 1)

Manufacturing

Manufacturing of modules with a programmable or a non-programmable chip is not different. A chip is placed and wire bonded in a cavity and a crystal blank is added. From the point of view of assembly, both are identical. However, the crystal for a programmable oscillator may be less expensive because you are more or less free to pick a frequency with the lowest overall cost and highest yield. All oscillator modules will use the same crystal frequency so the crystal manufacturing process can be optimized for this one crystal, further lowering cost. When the crystal fails, you lose the value of the whole module so a more reliable crystal lowers cost on the side of module yield.

Logistics

The programmable clock only gets its final output frequency after programming. Before programming, every module is the same. This means that inventory carries only one module part number. With a non-programmable oscillator there will be a dedicated crystal and therefore dedicated part number for each different frequency.

When a customer asks for a new frequency that has not been manufactured before, it is just a matter of programming to make it with a programmable clock. With a non-programmable clock it would be required to design a new frequency crystal which would take several weeks, possibly months.

The programming is an extra process step required. Usually it is combined with final testing so the impact on throughput is minimal. However it requires additional control of programming codes that a non-programmable oscillator won’t have. Some manufacturers of programmable clocks make their own equipment for programming and testing in volume production but there is also equipment commercially available.

In general you could say that it depends upon the type of market which approach is the best choice. When the market is very high volume with only a few frequencies and changes do not happen often, then the non-programmable clock will be the best choice. When the market requires a lot of different frequencies and there are often requests for new frequencies, then the programmable clock provides a much more flexible environment to react quickly to changes while maintaining a simple inventory with only one part number.

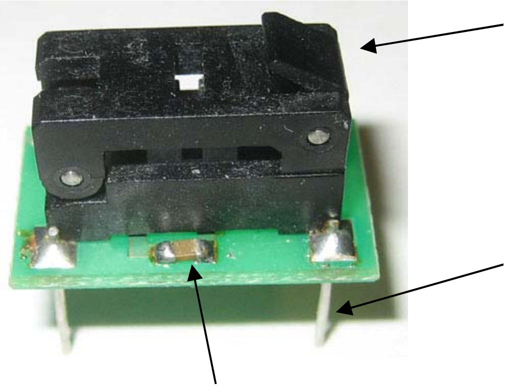
Testing during manufacturing

A programmable clock uses PLL architecture to synthesize the required output frequency from one crystal frequency. A PLL synthesizer needs good power supply decoupling for optimum performance. It has more complex circuitry and ripple on VDD caused by the output buffer driving the required load can interfere with the operation of the PLL. In this case the rule “the simpler, the better” really counts. A non-programmable clock circuit is so simple that noise on the power supply can not really interfere with its operation. So it is possible that old test equipment and test sockets designed for the old non-programmable clock modules do not pay much attention to power supply decoupling. As a result, the test equipment may say a module with a programmable clock is defective while it is not.

The higher sensitivity to power supply decoupling is not a problem for the end application because end users will always place decoupling near timing devices to maintain signal integrity and lower EMI through the whole circuit.

There is standard equipment available for testing oscillator modules like for example the Saunders 280A/B testers. This equipment usually has a textool socket for testing 14pin DIP and 8pin DIP size oscillator modules. These days most oscillator modules come in much smaller ceramic packages and small adaptor sockets are being used to be able to test ceramic modules with the common testers. When testing programmable clocks on this equipment it is essential that the adaptor socket has a power supply decoupling capacitor. Without this capacitor, the nearest decoupling is inside the tester which will be too far away to provide sufficient decoupling for a programmable clock. Appendix 1 shows oscilloscope pictures of good versus bad decoupling situations. The bad decoupling in appendix 1 has the capacitor at similar distance as when there is no decoupling on the adaptor. Appendix 1 will also explain further how VDD ripple occurs with bad decoupling.

Below is picture 1 of a properly decoupled adaptor.



Test socket for ceramic module.

4 pins to fit tester textool socket.

Power supply decoupling capacitor, 10nF ~ 100nF

(Picture 1)

Low VDD testing

Testing at different VDD voltages is another subject that often confuses users. A popular test for plain crystal oscillators, especially the 3rd overtone kind, is to check operation at a very low VDD voltage, much below the specified operating range. This is done to judge crystal oscillator gain margin. However, the programmable PL611s has a sophisticated startup procedure inside the chip and the output is enabled between 1.5V and 1.6V. This startup voltage of 1.5~1.6V does not say anything about crystal oscillator gain margin. In fact, the crystal oscillator itself usually already starts at about 1.0V. The low voltage test can not really be used with the PL611s. At best the operation can be verified at the low end of the specified operating range. For example, operation can be verified at 1.62V for the 1.8V operating voltage (1.8 – 10% = 1.62).

The programmable PL611s is specified for use from 1.8V to 3.3V operating voltages. However, programming certain settings can limit the usage to 3.3V operation only and the chip may not yet work at 1.62V. When programming settings limit usage to 3.3V only, then the lowest guaranteed operating voltage will be 2.97V. Programming settings for 2.5V operation guarantee operation at 2.25V and higher.

Frequency accuracy

The PL611s programmable clock has a frequency tuning capability through programming. For example, oscillator modules can be manufactured with a tolerance of ±20ppm at room temperature, before programming. When a customer places an order, modules are taken from inventory for programming / testing and then shipping. While programming, the frequency can be tuned, reducing the tolerance at room temperature to within ±5ppm.

Jitter and Phase Noise

The phase noise and jitter performance with a PLL are not as good as with a plain non-programmable crystal oscillator. For applications that require very good phase noise or jitter performance, the plain oscillator may be better. Typical period jitter performance of the PL611s is about 70ps PkPk. A plain crystal oscillator may show about 20ps PkPk. The PLL circuit increases phase noise in approximately the region 1KHz to 10MHz offset. The PL611s may show about -100dBc at 100KHz offset while a plain crystal oscillator may show as low as -140dBc at 100KHz offset. Close in, at 10Hz and 100Hz offsets the phase noise is about the same and also further out, at about 10MHz offset the results are about the same again between PL611s and a plain crystal oscillator. However, this type of phase noise performance is only important for very demanding applications like radio (wireless) or data communication where signal to noise ratios are important. Clocks for microprocessors or microcontrollers usually do not have phase noise requirements and the jitter of the PL611s is still good enough too.

Appendix 2 shows typical jitter and phase noise test results.

Compromise: Programmable non-PLL

PhaseLink has a PL610 chip that is programmable but without the PLL synthesizer. It has one programmable counter to divide down the crystal frequency to the output frequency. The division can be programmed between 1 and 63. There is no PLL so it has the good jitter and phase noise of the plain crystal oscillator. However, with only one counter it does not have the full flexibility of a PL611s but still better than a plain crystal oscillator. The programmable frequency tuning is the main reason customers are choosing the PL610 over other plain crystal oscillators.

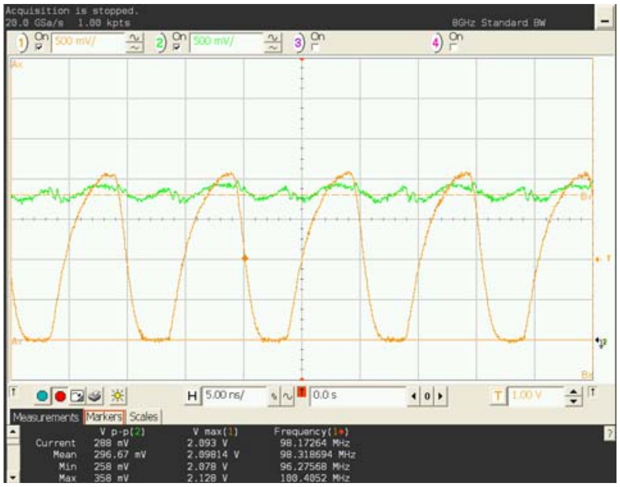
General conclusion:

The new programmable technology clocks offer improved flexibility while simplifying logistics and inventory. However, the PLL architecture of the programmable chips requires extra attention to test environment and desired noise performance.

Appendix 1: Good decoupling versus bad decoupling

A decoupling capacitor next to a chip is like local storage for power. When there is a sudden need for power, it can be tapped from the decoupling capacitor. When there is no decoupling nearby the chip and there is a sudden need for power, the VDD on the chip will drop for a short time until the power from further away arrives at the chip. In clock chips a sudden need for power happens on the rising edge of the output signal, where the output load needs to be charged quickly with current flowing from the VDD rail. The pictures below show the output signal from a PL611s with 15pF load in two situations: “Bad” and “Good” decoupling. With bad decoupling, the capacitor is placed at 30mm distance from the chip. With good decoupling the distance was only 2mm. The distance is the main contributor to making decoupling “bad”.

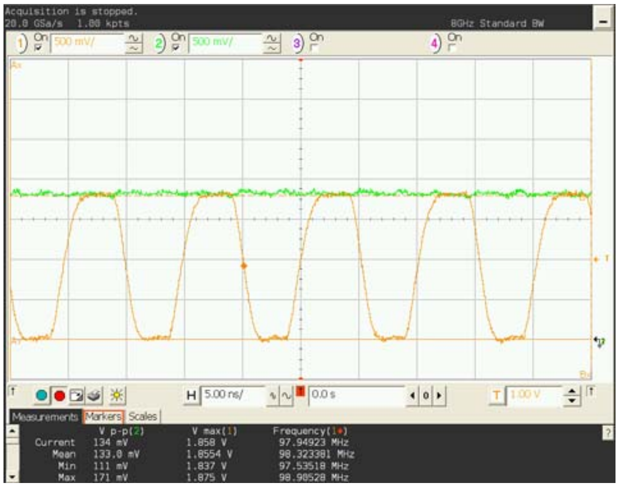
VDD=1.8V, Bad decoupling:



```
Acquisition is stopped.
20.0 GSa/s  1.00 kpts                     8GHz Standard BW

          V p-p(2)      V max(1)     Frequency(1)
Current   288 mV        2.093 V       98.17264 MHz
   Mean   296.67 mV     2.09814 V     98.318694 MHz
    Min   258 mV        2.078 V       96.27568 MHz
    Max   358 mV        2.128 V       100.4052 MHz
```

VDD=1.8V, Good decoupling:



```
Acquisition is stopped.
20.0 GSa/s  1.00 kpts                     8GHz Standard BW

          V p-p(2)      V max(1)     Frequency(1)
Current   134 mV        1.858 V       97.94923 MHz
   Mean   133.0 mV      1.8554 V      98.323381 MHz
    Min   111 mV        1.837 V       97.53518 MHz
    Max   171 mV        1.875 V       98.98528 MHz
```

The yellow trace is the output waveform and the green trace is the VDD pin of the PL611s. The most obvious result of the bad decoupling in this case (1.8V) is a slower rising edge.

VDD=2.5V, Bad decoupling:

```
Acquisition is stopped.
20.0 GSa/s   1.00 kpts                                  8GHz Standard BW

          V p-p(2)     V max(1)     Frequency(1*)
Current   644 mV       2.961 V      97.71639 MHz
   Mean   633.2 mV     2.9784 V     98.351167 MHz
    Min   565 mV       2.945 V      96.20886 MHz
    Max   981 mV       3.210 V      100.5204 MHz
```

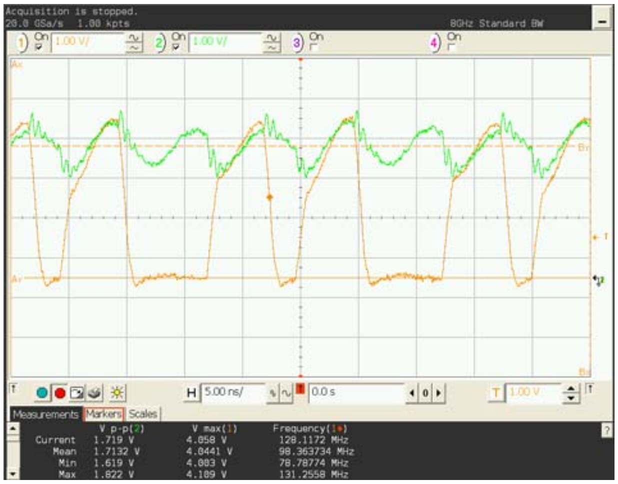
VDD=2.5V, Good decoupling:

```
Acquisition is stopped.
20.0 GSa/s   1.00 kpts                                  8GHz Standard BW

          V p-p(2)     V max(1)     Frequency(1*)
Current   165 mV       2.585 V      98.46279 MHz
   Mean   177.5 mV     2.5841 V     98.324639 MHz
    Min   153 mV       2.566 V      98.02620 MHz
    Max   236 mV       2.625 V      98.66342 MHz
```

At VDD=2.5V the situation gets a bit worse compared to 1.8V because the output buffer is a bit stronger and demands a bigger current from VDD to charge the output load.

VDD=3.3V, Bad decoupling:



```
Acquisition is stopped.
20.0 GSa/s   1.00 kpts                                  8GHz Standard BW

          V p-p(2)     V max(1)     Frequency(1*)
Current   1.719 V      4.058 V      128.1172 MHz
   Mean   1.7132 V     4.0441 V     98.363734 MHz
    Min   1.619 V      4.003 V      78.78774 MHz
    Max   1.822 V      4.189 V      131.2558 MHz
```

VDD=3.3V, Good decoupling:

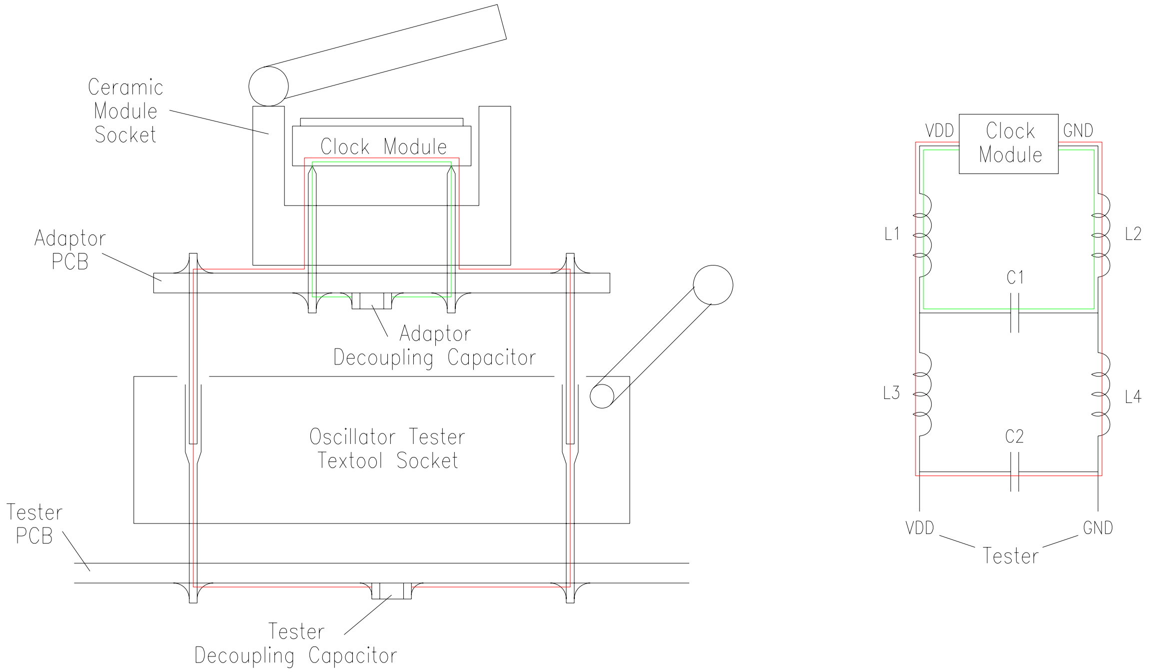
```
Acquisition is stopped.
20.0 GSa/s   1.00 kpts                                  8GHz Standard BW

          V p-p(2)     V max(1)     Frequency(1*)
Current   230 mV       3.478 V      98.38484 MHz
   Mean   249.7 mV     3.4644 V     98.320582 MHz
    Min   218 mV       3.442 V      98.00712 MHz
    Max   291 mV       3.495 V      98.60215 MHz
```

With bad decoupling, at VDD=3.3V the ripple on VDD becomes so large that the PLL is losing lock. On the rising edge, the VDD collapses to about 2.5V. The total ripple is 1.7Vpp in this case.

If the test equipment decoupling would be as bad as this case, then it would report a defect with a wrong output frequency. This loss of lock does not happen with a non-programmable oscillator because it generally does not have a PLL but it will have the same issues with the rising edge and will still show a somewhat distorted output signal.

More details about VDD ripple



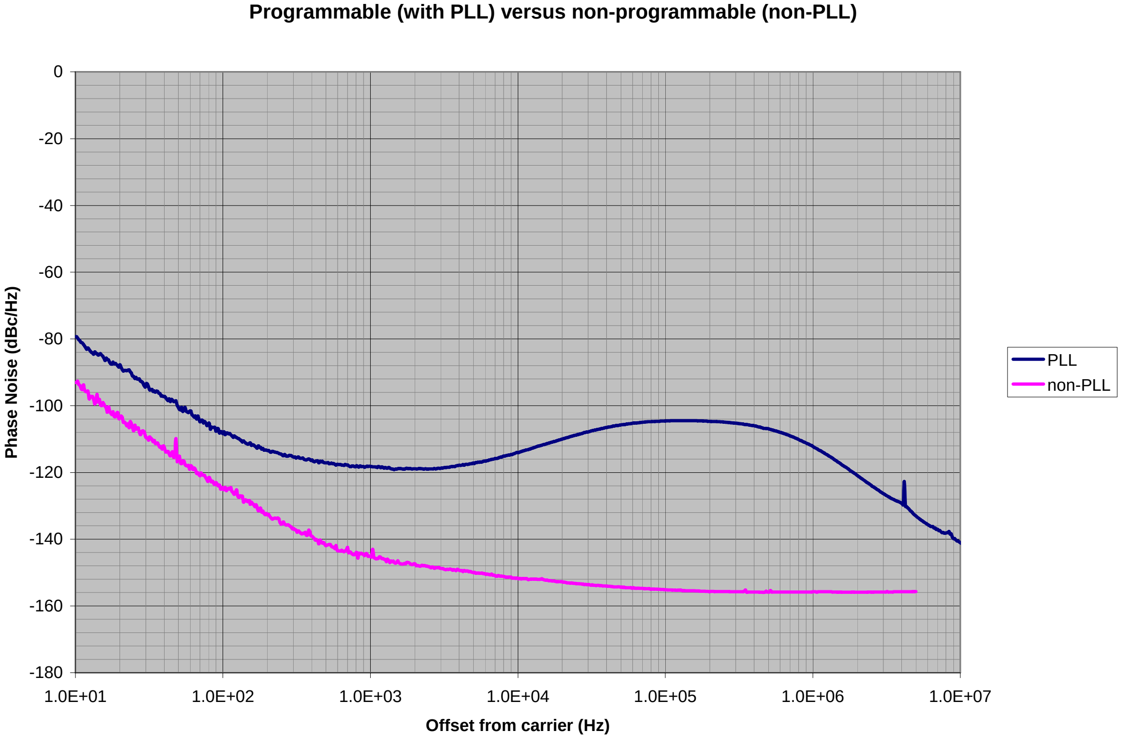
(Diagram 2)

When clock oscillator modules are tested with a tester like the Saunders 280A/B, an adaptor is needed to fit the ceramic module type. When there is no adaptor decoupling capacitor (C1) then the path to the next available decoupling capacitor in the tester (C2) is very long. In above drawings the red path is when the adaptor decoupling capacitor is missing and the green path is when the adaptor decoupling capacitor is present. It is obvious that the red path is much longer and will cause a situation of bad decoupling for programmable clock modules.

The length of pins and PCB traces can be represented with inductors. L1 and L2 are estimated to be about 10nH each. L3 and L4 are estimated to be about 40nH each. C1 and C2 will buffer the voltage so the ripple across C1 and C2 is almost zero. When C1 is present, the ripple between VDD and GND at the clock module is low because there is only L1 and L2 (20nH total) until the closest decoupling capacitor (C1). When C1 is not present the ripple can be about five times larger because the total inductance between module and the next available decoupling capacitor is now about 100nH.

The requirements for the adaptor decoupling capacitor C1 are a high enough value to be a good buffer and good high frequency properties to react quickly to sudden demands for power. Ceramic capacitors with size 0603 or 0805 and with material X7R or Y5V have good high frequency properties. The most commonly used value is 0.1µF.

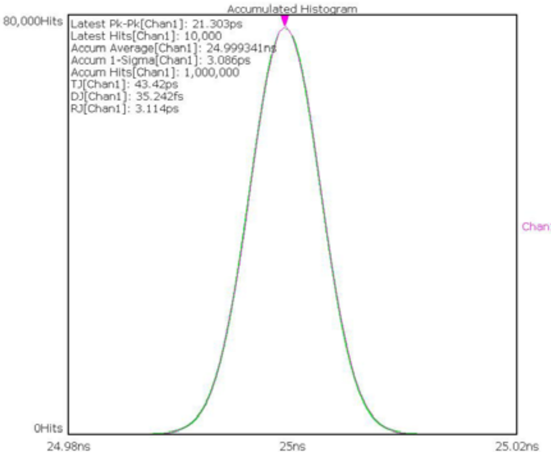
Appendix 2: Typical Phase Noise performance



The PLL creates a region of increased phase noise, approximately between 1KHz and 10MHz offsets from the carrier.

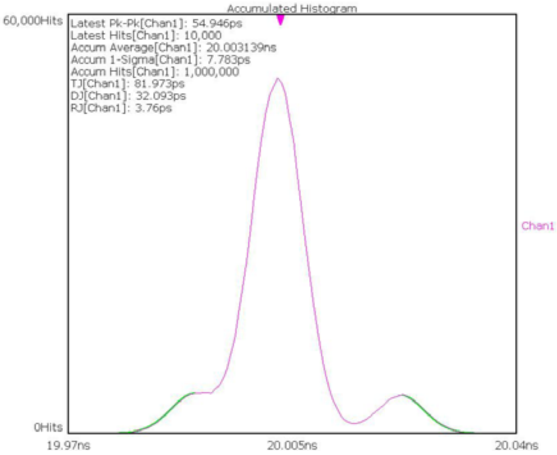
Typical Jitter Performance

Non-programmable (non-PLL):



```
Latest Pk-Pk[Chan1]: 21.303ps
Latest Hits[Chan1]: 10,000
Accum Average[Chan1]: 24.999341ns
Accum 1-Sigma[Chan1]: 3.086ps
Accum Hits[Chan1]: 1,000,000
TJ[Chan1]: 43.42ps
DJ[Chan1]: 35.242fs
RJ[Chan1]: 3.114ps
```

Programmable (with PLL):



```
Latest Pk-Pk[Chan1]: 54.946ps
Latest Hits[Chan1]: 10,000
Accum Average[Chan1]: 20.003139ns
Accum 1-Sigma[Chan1]: 7.783ps
Accum Hits[Chan1]: 1,000,000
TJ[Chan1]: 81.973ps
DJ[Chan1]: 32.093ps
RJ[Chan1]: 3.76ps
```

The main difference between the two period jitter histograms is the additional “deterministic jitter” (DJ) with the programmable clock oscillator with a PLL synthesizer.