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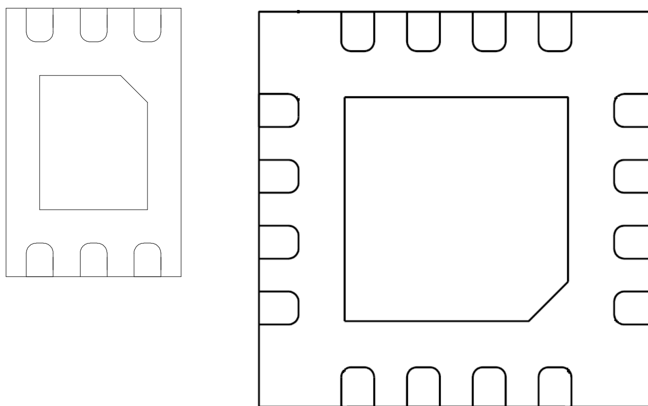
The DFN and QFN packages of the PhaseLink IC's have a large solder pad in the middle. The official function of this pad is to aid thermal conductivity from the chip to the PCB to lower the thermal resistance Tja. The general name for this pad is the "thermal relief pad".

Below is the bottom view of the DFN-6L (2.0x1.3mm) and the QFN-16L (3x3mm).

Figure 1: DFN-6L QFN-16L



The thermal relief pad is an exposed area of the leadframe inside the IC. The chip is assembled on the flipside of the pad, inside the package. When the pad is soldered to the PCB there is a low thermal resistance between the chip and the PCB. The thermal resistance Tja is in the 20~30°C/Watt range.

All PhaseLink clock chips in DFN-6L are low power chips that do not really need thermal relief. There are a number of high frequency chips with LVPECL outputs in QFN-16L that require the use of the thermal relief pad.

When making an electrical connection to the thermal relief pad, this connection needs to be power ground. More specifically, the pad needs to be connected to the lowest DC potential to the IC, which are either GND pins or VSS/VEE pins.

There are two choices for the thermal relief pad:

1) Solder the pad to the PCB for thermal relief. In this case the solder pad for the thermal relief pad needs to be connected to power ground.
2) Don't solder the thermal relief pad. For this case make sure there is solder mask below the IC so the thermal relief pad does not connect to potential traces running under the IC.

The threshold for considering thermal relief is roughly 100mW. If the expected power dissipation is bigger than 100mW then it is advised to solder the thermal relief pad.