

## PL602-2X PCB Design Recommendations

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The PL602-2X series of products is a small synthesizer to generate clocks with HCSL logic levels for the PCI express interface. Each PL602-2X can drive either one or two differential HCSL clock lines.

The PL602-2X output pins actually swing rail-to-rail (0V~VDD) and HCSL levels are achieved through selection of the proper value series resistor.

Figure 1: Output Schematic for driving one Differential Output.

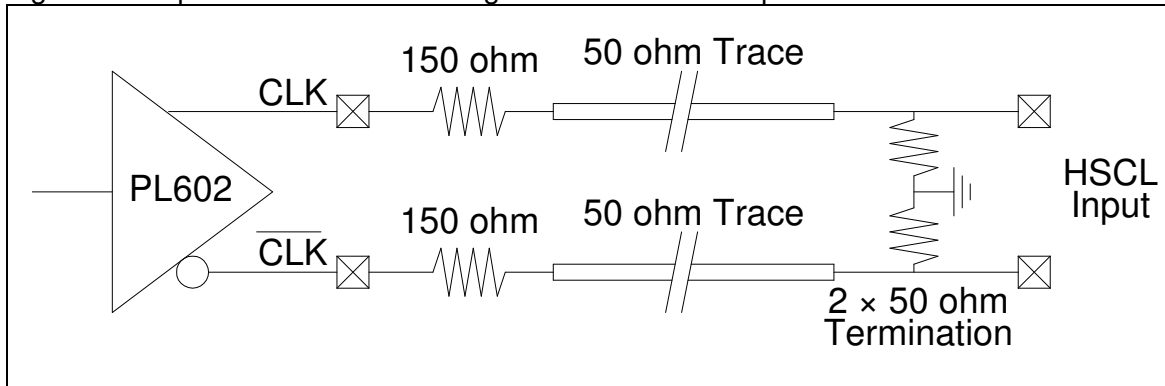
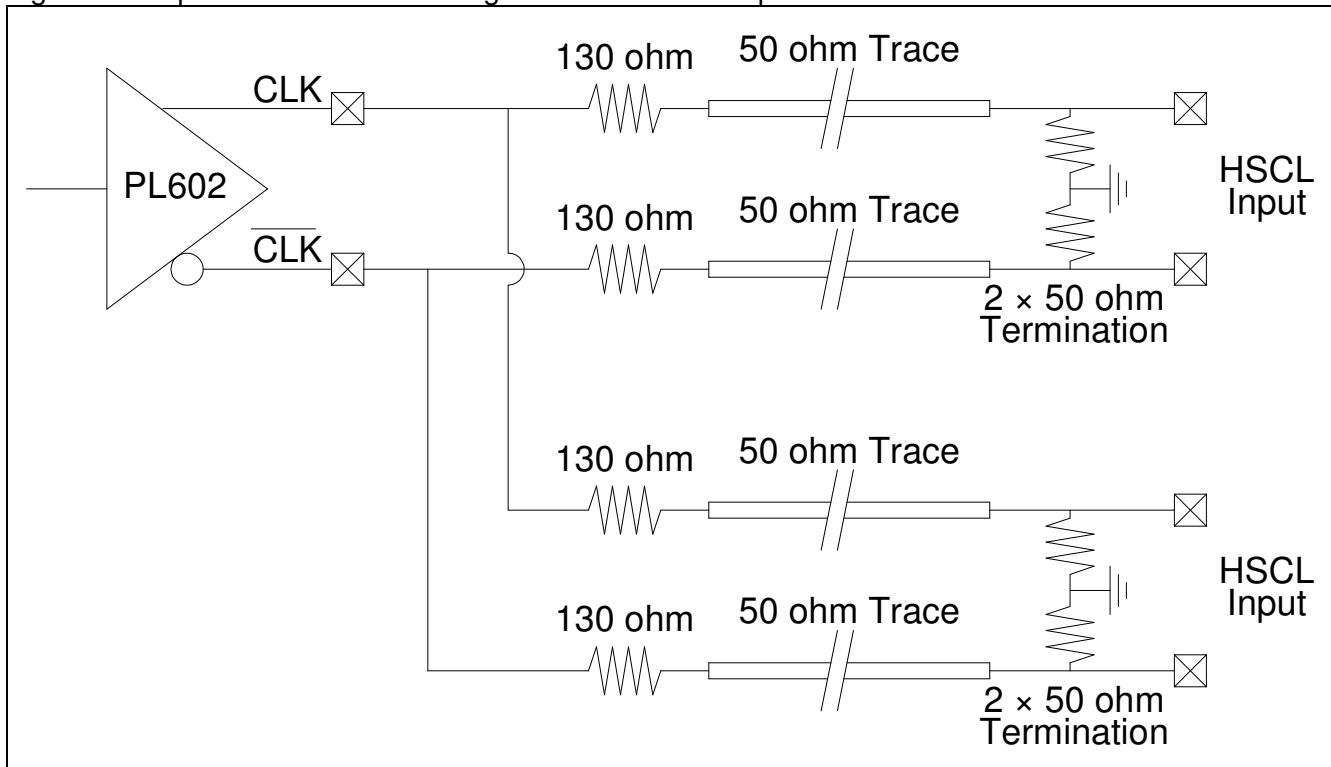
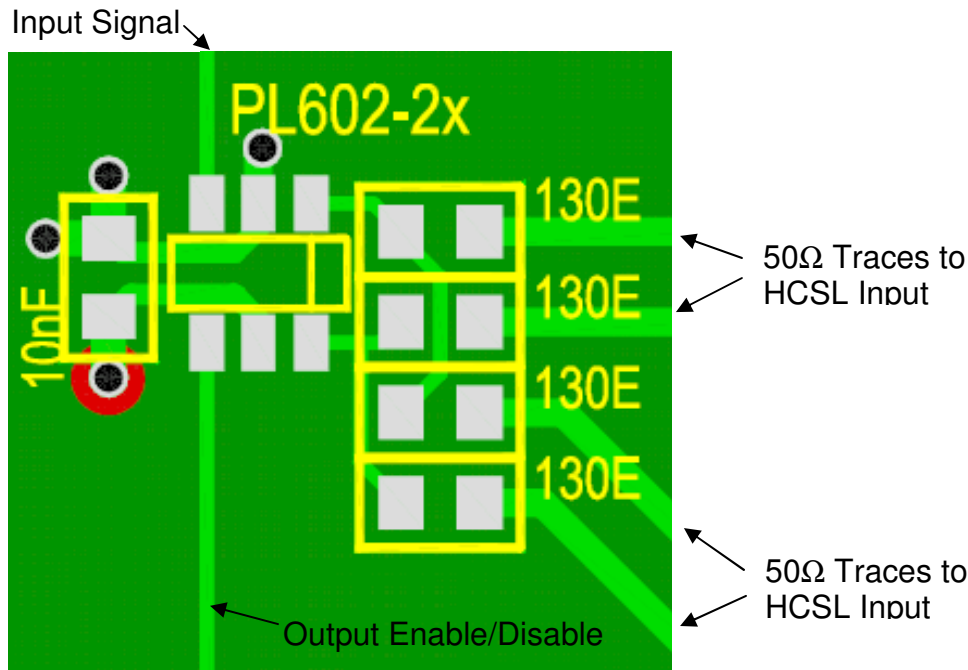


Figure 2: Output Schematic for driving two Differential Outputs.



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Figure 3: Example PCB Design for driving two Differential Outputs.



**PCB Design Considerations:**

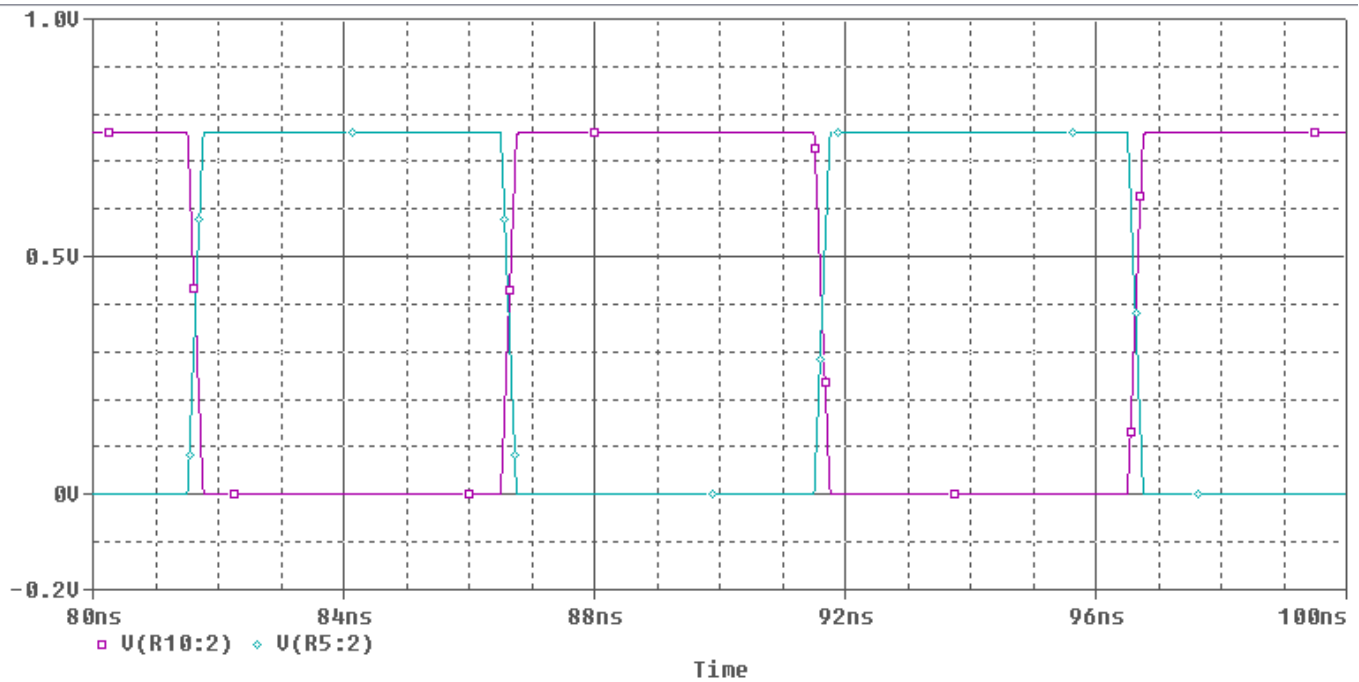
- The PL602-2X is a PLL synthesizer and power supply decoupling is important for good period jitter performance. Place a 0.01μF ~ 0.1μF capacitor as close as possible to the GND and VDD pins of the IC. It is advised to route traces from the decoupling capacitor directly to the power pins on the IC, without going through vias. The goal is to make the power supply impedance as low as possible for high frequencies.
- The series resistors for the outputs need to be as close as possible to these outputs with as short as possible PCB traces for the best signal integrity of the output signal.
- Design pairs of 50Ω traces to bring the clock signal to its target HCSL input. It is advised to maintain a 50Ω impedance as well as possible along the full length of the trace and avoid as much as possible interruptions of the 50Ω impedance like vias and sharp corners.
- Trace length equals time. To maintain good skew between the two traces for the differential signal, it is very important that the traces have equal length. A typical requirement for this skew is < 50ps. This means no more than 10mm difference in effective length between the two traces for the differential signal. Actually, 10mm is a relatively large number so skew issues are unlikely to happen.
- In case the skew between the two differential pairs from one PL602-2X is also important then also make sure that the length of the pairs is equal. The speed in PCB traces is roughly 5ps/mm so for example when the skew needs to be within 200ps, the difference in length should be less than 40mm.

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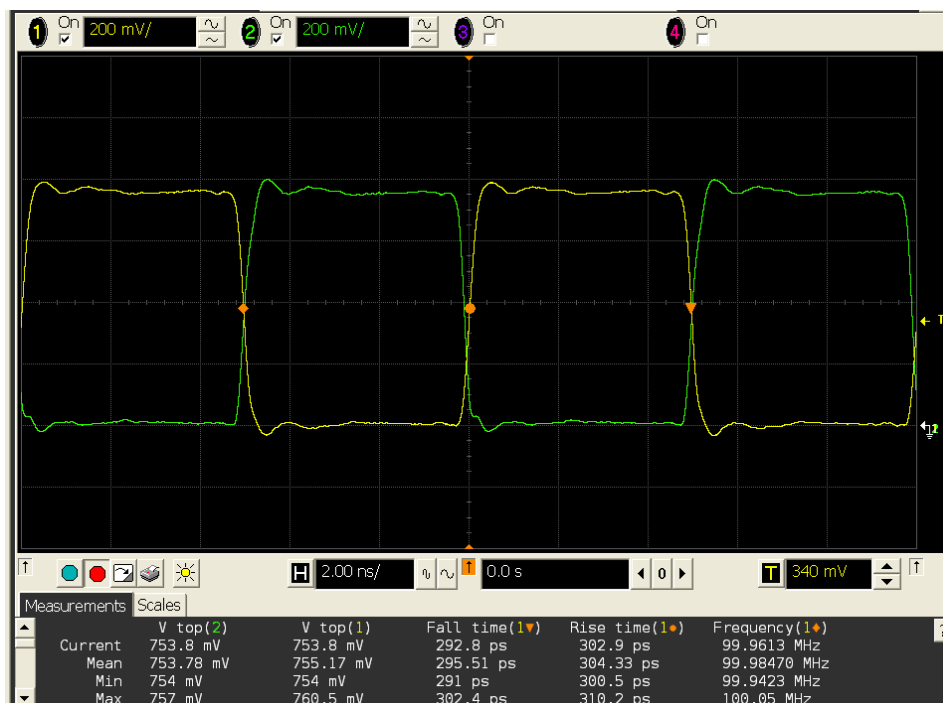
### Breaking the rules

When the above guidelines are not followed there will be consequences for skew or signal integrity. In this chapter I will show some of these consequences and try to find how far a certain rule can be bent before things really get out of control.

The perfect waveform looks like this (simulated):

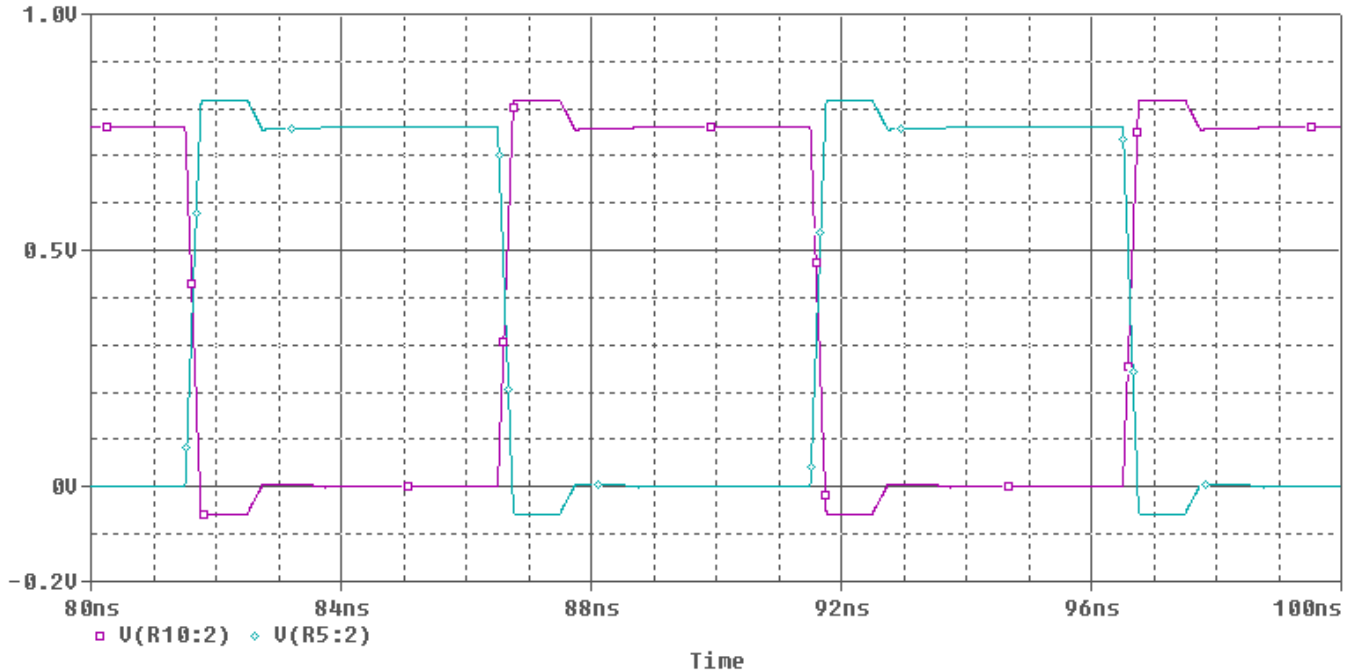


This is an actual measurement of a PL602-21:

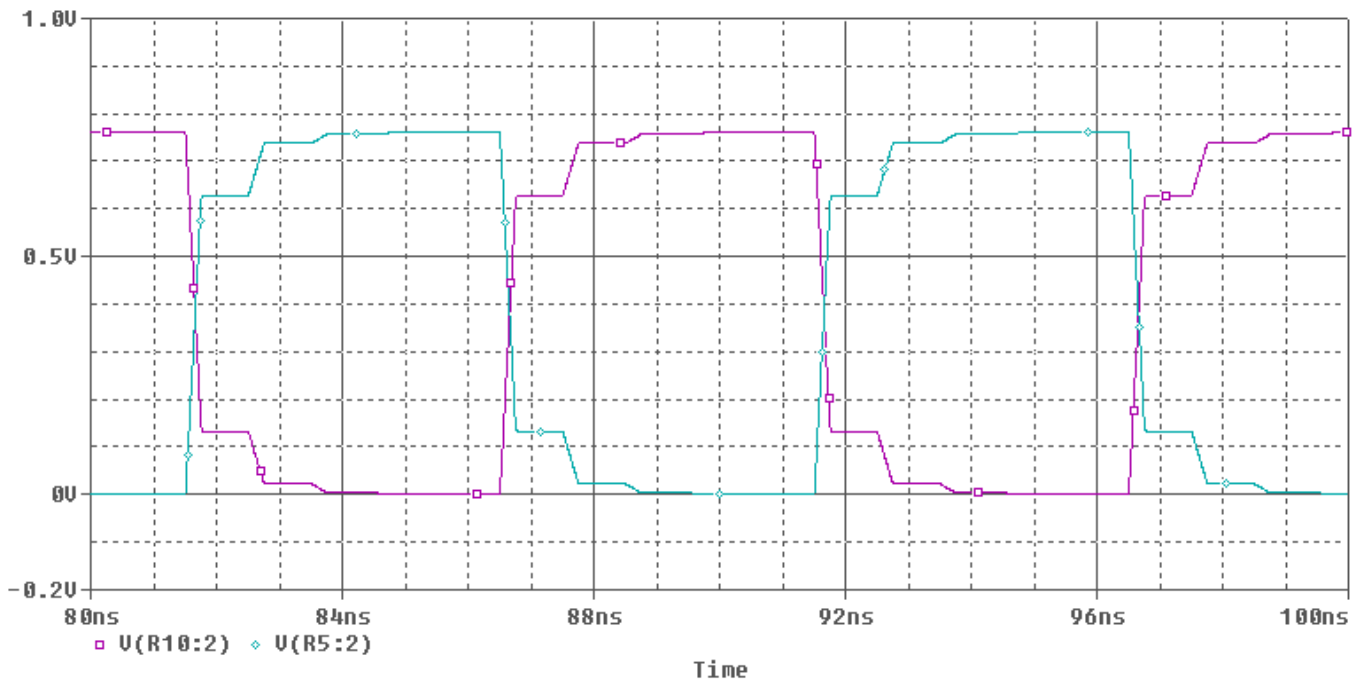


### Improper Trace Impedance

When the trace impedance is not 50Ω then there will be reflections. The first plot is with a trace impedance of 75Ω.



The next plot is with a trace impedance of 30Ω.

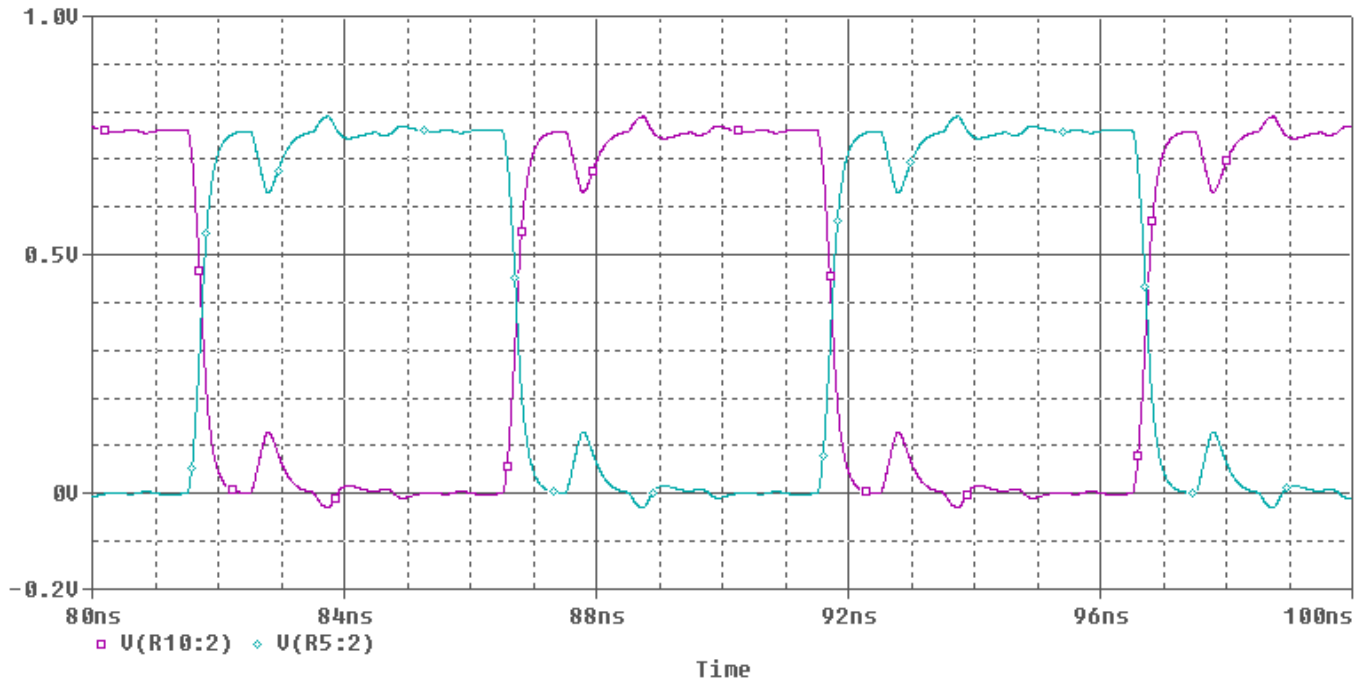


The reflections from these large trace impedance errors ( $\pm 50\%$  errors) are not that bad. This design is quite robust versus trace impedance errors. When a similar impedance error happens for only part of the trace, the impact will be even less.

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### Capacitive Loading at the HCSL Input

When the HCSL input pins has a significant amount of (parasitic) capacitance, either in the PCB or inside the chip, there will be reflections and/or ringing. Below plot was simulated with 5pF capacitance at both HCSL inputs.

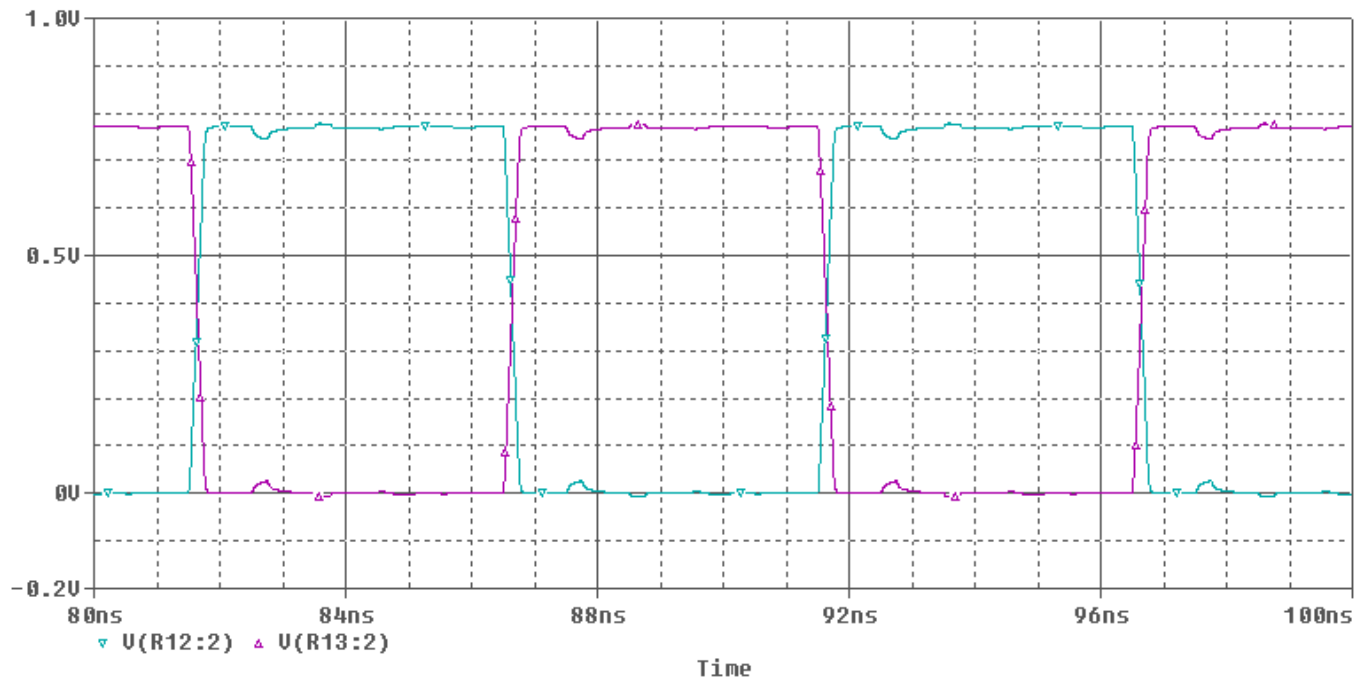
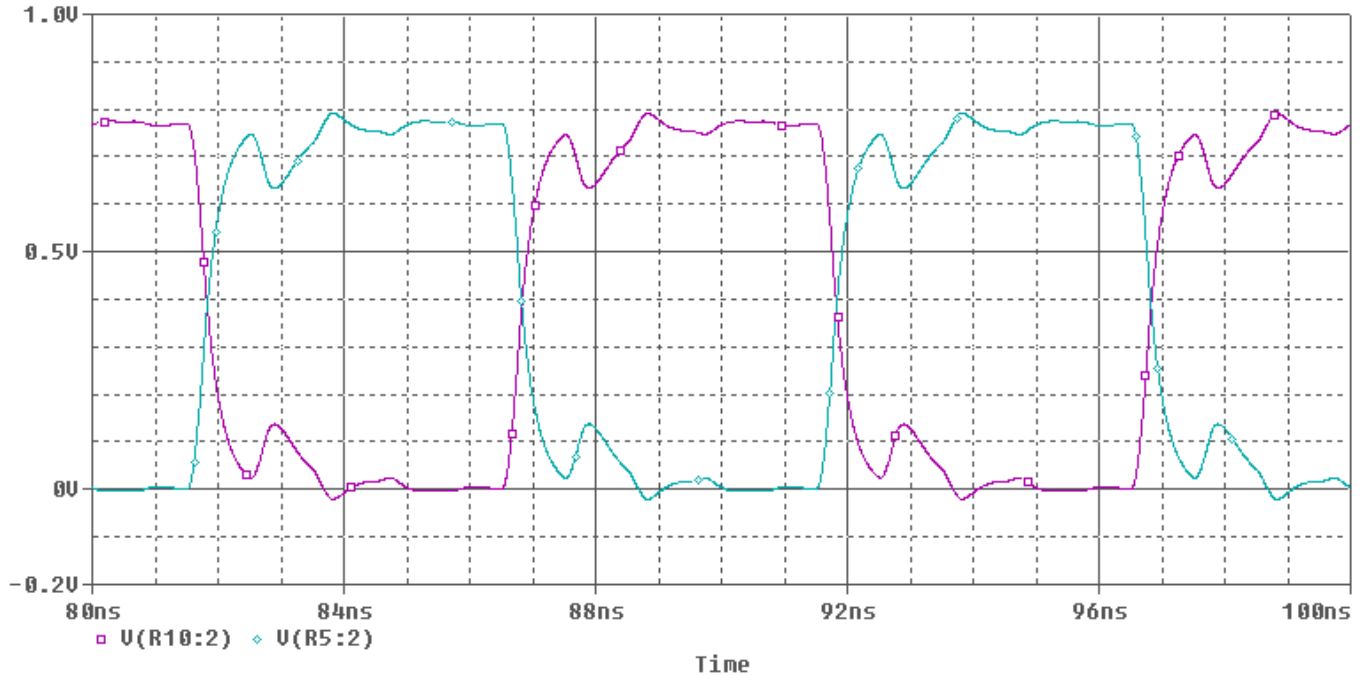


5pF is a lot of capacitance and the reflections do not yet get close to the signal threshold. This means that the circuit can tolerate a significant amount of capacitance at the side of the HCSL inputs.

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### Interaction between Outputs when driving two sets of Differential Outputs

When driving two differential pairs of traces and one side has some kind of a problem, some of the trouble on that one side will also affect the other pair. The first plot below shows the results of 10pF of parasitic capacitance on one differential pair and the next plot shows how much this affects the other differential pair with 'perfect' termination.



You can see how there is a small reaction in the lower plot to the trouble in the upper plot. Theoretically the isolation between the two differential pairs is about 30dB.