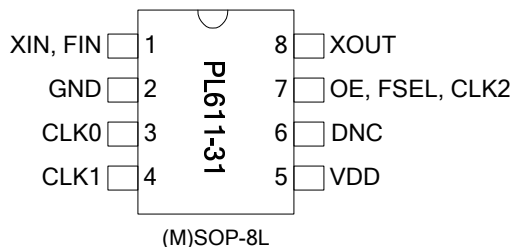


FEATURES

- Advanced programmable PLL design
- Very low Jitter and Phase Noise (< 40ps Pk-Pk typical)
- Up to 3 outputs
- Output frequency up to 200MHz CMOS.
 - Provides complementary LVCMOS outputs to drive LVCMOS, LVPECL or LVDS inputs.
- Input frequencies:
 - Fundamental crystal: 10MHz - 30MHz
 - Reference Clock: 1MHz - 200MHz
- Accepts <1.0V reference signal input voltage
- One programmable I/O pin can be configured as Output Enable (OE) input, Frequency Selection (FSEL) input or Reference clock output.
- Single 2.5V ~ 3.3V ± 10% power supply
- Operating temperature range from -40°C to 85°C
- Available in 8-pin MSOP/SOP GREEN/RoHS compliant packages.

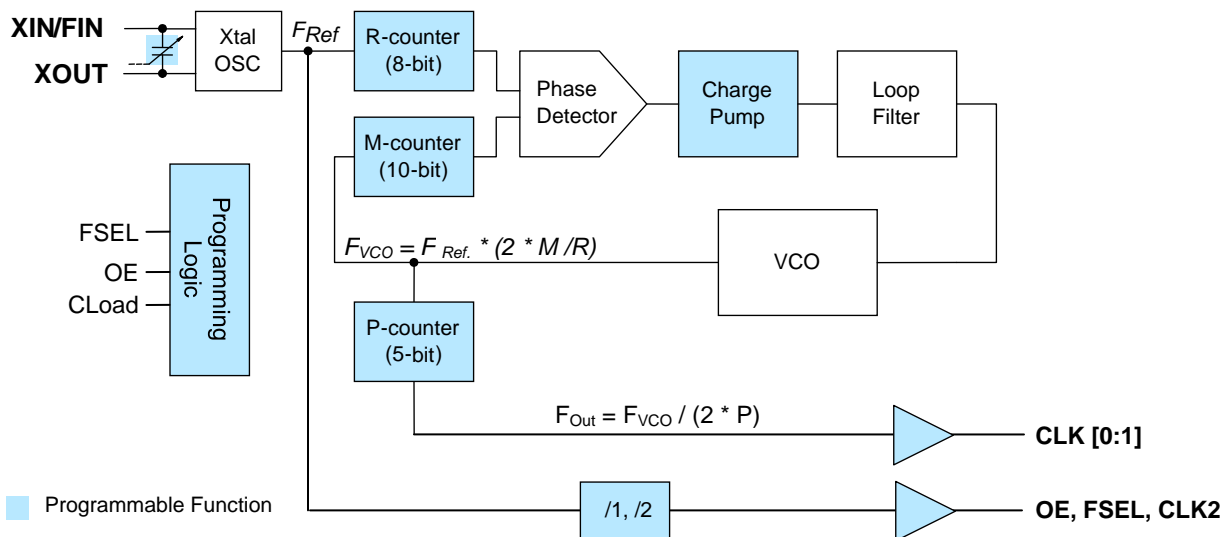
PIN CONFIGURATION



DESCRIPTION

The PL611-31 is a low-cost general purpose frequency synthesizer and a member of PhaseLink’s Factory Programmable ‘Quick Turn Clock (QTC)’ family. PhaseLink’s PL611-31 product family can generate any output frequency up to 200 MHz from a fundamental crystal input of 10MHz to 30MHz. In addition, the complementary LVCMOS outputs can be used to drive differential LVPECL or LVDS inputs at 2.5V or 3.3V

BLOCK DIAGRAM



Programmable Quick Turn Clock™
KEY PROGRAMMING PARAMETERS

CLK[0:2] Output Frequency	Output Drive Strength	Crystal Load	Programmable Input/Output (pin #7)	# of Register Banks
$F_{OUT} = F_{IN} * M / (R * P)$ where M=10 bit R = 8 bit P = 5 bit 1. CLK[0:1] = VCO / 2 * P 2. CLK0 = ~ CLK1 2. CLK[2] = F_{IN} or $F_{IN}/2$	Std: 10mA (default) High: 24mA	+/- 200ppm tuning	One output pin can be configured as 1. CLK2 - output 2. FSEL - input 3. OE - input	2

PIN DESCRIPTION

Name	Pin #	Type	Description									
	(M)SOP-8L											
XIN, FIN	1	I	Crystal or Reference input pin									
GND	2	P	GND connection									
CLK[0:1]	3,4	O	Programmable Clock Output [note:CLK0=CLK1]									
VDD	5	P	VDD connection (2.25~3.63V)									
DNC	6	-	Do No Connect									
OE, FSEL, CLK2	7	B	This programmable I/O pin can be configured as Output Enable (OE) input, Frequency Selection (FSEL) input or CLK2 (F_{IN} or $F_{IN}/2$) output. This pin has an internal 60KΩ pull up resistor. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>State</th> <th>OE</th> <th>FSEL</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Tristate CLK[0:1]</td> <td>Bank 0</td> </tr> <tr> <td>1 (default)</td> <td>Normal mode</td> <td>Bank 1</td> </tr> </tbody> </table>	State	OE	FSEL	0	Tristate CLK[0:1]	Bank 0	1 (default)	Normal mode	Bank 1
State	OE	FSEL										
0	Tristate CLK[0:1]	Bank 0										
1 (default)	Normal mode	Bank 1										
XOUT	8	O	Crystal output pin									

Programmable Quick Turn Clock™
ELECTRICAL SPECIFICATIONS
ABSOLUTE MAXIMUM RATINGS

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage Range	V_{DD}	-0.5	4.6	V
Input Voltage Range	V_I	-0.5	$V_{DD}+0.5$	V
Output Voltage Range	V_O	-0.5	$V_{DD}+0.5$	V
Data Retention @ 85° C		10		Years
Soldering Temperature (Green Package)			260	°C
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*		-40	+85	°C

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. *Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

AC SPECIFICATIONS

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Input Frequency	Fundamental Crystal	10		30	MHz
Input (F_{IN}) Frequency				200	MHz
Input (F_{IN}) Signal Amplitude	Internally AC coupled	0.9		V_{DD}	Vpp
Settling Time	At power-up ($V_{DD} \leq 1.62V$)			10	ms
VDD Sensitivity	Frequency vs. $V_{DD} \pm 10\%$	-2		2	ppm
Output Rise Time	15pF Load, 10/90% V_{DD} , Standard drive		2.5	3.5	ns
	15pF Load, 10/90% V_{DD} , High drive		1.0	1.5	ns
Output Fall Time	15pF Load, 90/10% V_{DD} , Standard drive		2.5	3.5	ns
	15pF Load, 90/10% V_{DD} , High drive		1.0	1.5	ns
Duty Cycle	At $V_{DD}/2$	45	50	55	%
Max. output skew between same frequency clocks	Equal loading (15 pF). Equal frequency & drive strength			200	ps
Period Jitter, peak-to-peak* (10,000 samples measured)	With capacitive decoupling between V_{DD} and GND. CLK0 & CLK1 active		40		ps

* Note: Jitter performance depends on the programming parameters.

Programmable Quick Turn Clock™
DC SPECIFICATIONS

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic, with Loaded Outputs	I_{DD}	At 10MHz, load=15pF			15	mA
Operating Voltage	V_{DD}		2.25		3.63	V
Output Low Voltage	V_{OL}	$I_{OL} = +4mA$ (Standard Drive)			0.4	V
Output High Voltage	V_{OH}	$I_{OH} = -4mA$ (Standard Drive)	$V_{DD} - 0.4$			V
Output Current	I_{OSD}	$V_{OL} = 0.4V, V_{OH} = 2.4V$ (Std Drive)		10		mA
	I_{OHD}	$V_{OL} = 0.4V, V_{OH} = 2.4V$ (High Drive)		24		mA
Short-Circuit Current	I_S			±50		mA

CRYSTAL SPECIFICATIONS

PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNITS
Fundamental Crystal Resonator Frequency	F_{XIN}	10		30	MHz
Crystal Loading Rating (The IC can be programmed for any value in this range.)	C_L (xtal)	5		20	pF
Maximum Sustainable Drive Level				500	μW
Operating Drive Level			100		μW
Crystal Shunt Capacitance	C_0			6	pF
Effective Series Resistance, Fundamental, 10-30MHz	R_s			30	Ω
Effective Series Resistance, 3 rd Overtone, 30-50MHz [$C_0 < 4pF, C_L = 5pF/8pF$]	ESR			100/70	Ω
Effective Series Resistance, 3 rd Overtone, 50-65MHz, [$C_0 < 4pF, C_L = 5pF/8pF$]	ESR			60/40	Ω
Effective Series Resistance, 3 rd Overtone, 65-75MHz [$C_0 < 4pF, C_L = 5pF/8pF$]	ESR			45/30	Ω

TERMINATING COMPLEMENTARY LVCMOS OUTPUTS

Figure 1 below describes how to terminate the complementary LVCMOS outputs of PhaseLink's PL611-31 Programmable QTC clock for use with LVPECL or LVDS inputs.

The unique feature of complementary LVCMOS outputs allows great flexibility for board designers. By standardizing on one termination scheme you can use the PL611-31 for all your LVDS and LVPECL clock requirements up to 200MHz.

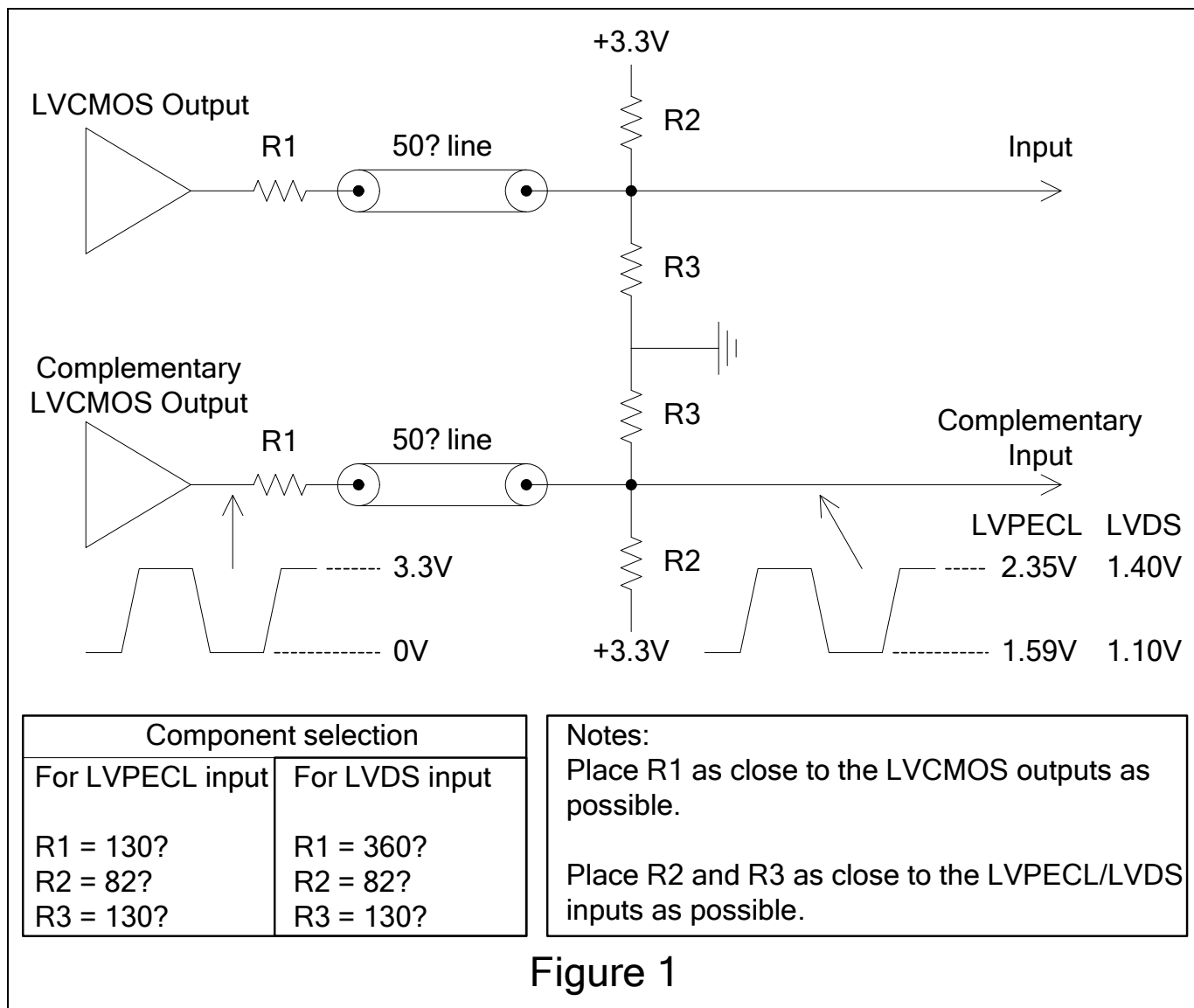


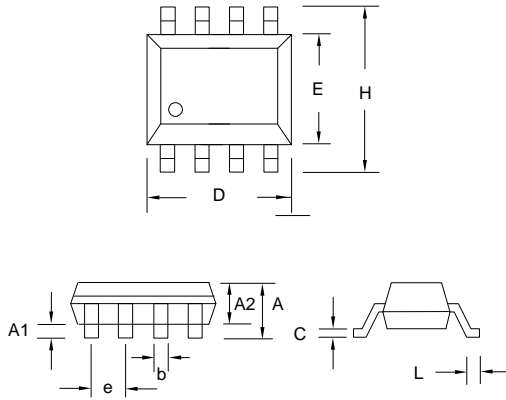
Figure 1

The above layout allows the PL611-31 to drive either an LVPECL or LVDS input pair by simply changing the value of R1.

PACKAGE DRAWINGS (GREEN PACKAGE COMPLIANT)

MSOP-8L

Symbol	Dimension in MM	
	Min.	Max.
A	---	1.10
A1	0.05	0.15
A2	0.81	0.91
B	0.25	0.40
C	0.13	0.23
D	2.90	3.10
E	2.90	3.10
H	4.90 BSC	
L	0.445	0.648
e	0.65 BSC	



SOP-8L

Symbol	Dimension in MM	
	Min.	Max.
A	1.35	1.75
A1	0.10	0.25
A2	1.25	1.50
B	0.33	0.53
C	0.19	0.27
D	4.80	5.00
E	3.80	4.00
H	5.80	6.20
L	0.40	0.89
e	1.27 BSC	

