

1.8V-3.3V PicoPLL™ Programmable Quick Turn Clock™

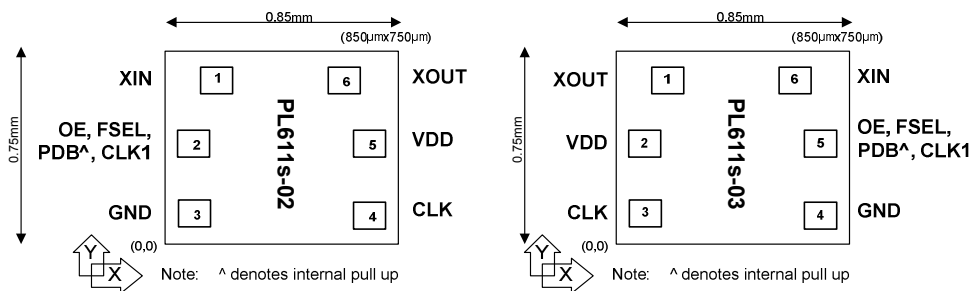
FEATURES

- Advanced One Time Programmable PLL design.
- Programmable PLL or Direct Oscillation operation.
- Very low Jitter and Phase Noise (30-70ps Pk-Pk typical)
- Output frequency range
 - ≤110MHz @ 1.8V operation
 - ≤166MHz @ 2.5V operation
 - ≤200MHz @ 3.3V operation
- Input Frequency: Fundamental crystal: 10MHz-50MHz.
- 8bit Switch Capacitor for ±50ppm crystal C_L tuning.
- Low current consumption, <10μA when PDB is activated.
- One programmable I/O pin can be configured as Output Enable (OE) or Power Down (PDB) input.
- Single 1.8V, 2.5V, or 3.3V ± 10% power supply
- Operating temperature range from -40°C to 85°C
- Wire bond (-02) or Flip-Chip (-03) pad layout.

DESCRIPTION

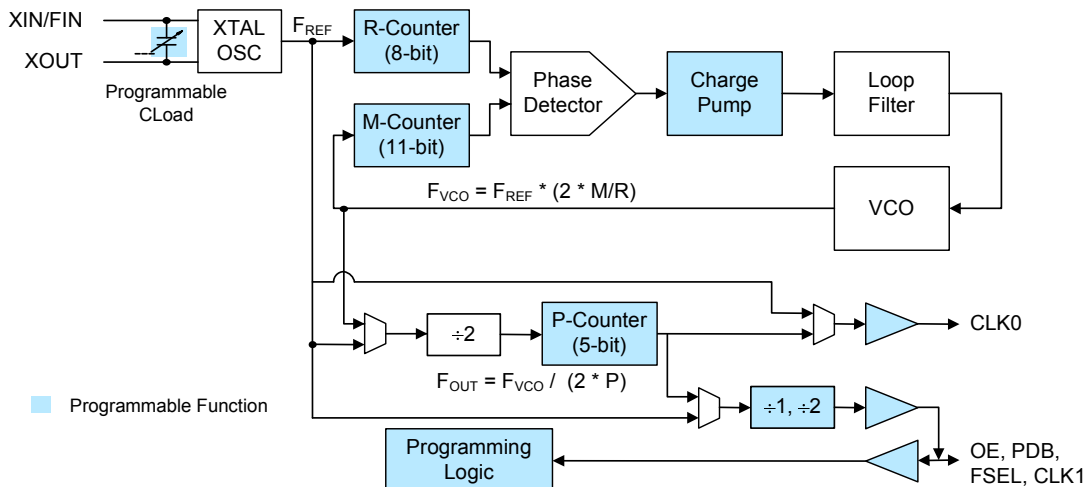
The PL611s is a high performance low-cost general purpose frequency synthesizer and a member of PhaseLink's PicoPLL™ Factory Programmable 'Quick Turn Clock (QTC)'. Designed to fit in a small 2.5mmx2.0mm oscillator module for high performance applications, the PL611s offers the best phase noise and jitter performance, smallest die size, and power consumption of any comparable device. The power down feature of PL611s, when activated, allows the IC to consume less than 10μA of power, while its programming flexibility allows generating any output, using a low-cost crystal input.

PAD CONFIGURATION & DIE SPECIFICATION



Parameter	Value
Chip size	0.75 x 0.85mm
Chip thickness	<150-250μm
Pad size	90μm
Chip base	GND level

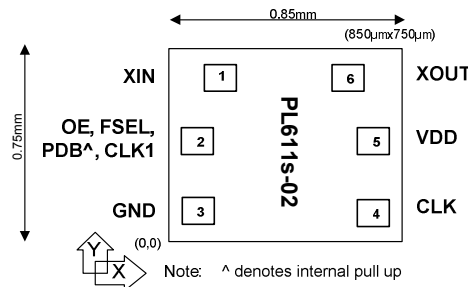
BLOCK DIAGRAM



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KEY PROGRAMMING PARAMETERS

Output Frequency	Output Drive Strength	Crystal Load	Programmable Input/Output	Charge-Pump Current
<p>CLK0 PLL Mode : $CLK0 = F_{IN} * M / (R * P)$ Where: <ul style="list-style-type: none"> M=11 bit R= 8 bit P= 5 bit P is an Odd/Even Divider Direct Oscillation Mode: $CLK0 = F_{IN}$ or $F_{IN} / (2 * P)$ CLK1 = F_{IN}, $F_{IN}/2$, CLK0 or CLK0/2</p>	<p>Three optional drives to choose from. They are:</p> <ul style="list-style-type: none"> Low: 4mA Std: 8mA (default) High: 16mA 	<p>Programmable CLoad Tuning</p> <ul style="list-style-type: none"> 8pF to 12pF ±50ppm typical 	<p>One pad can be configured as:</p> <ul style="list-style-type: none"> OE – input PDB – input FSEL – input CLK1 – output 	<p>Charge pump current</p> <ul style="list-style-type: none"> 4 levels; programmable

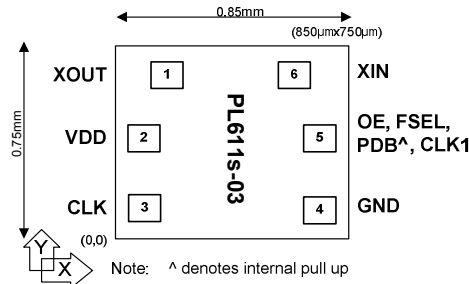


PAD ASSIGNMENT AND DESCRIPTION (PL611s-02)

Name	Pad Assignment*			Type	Description												
	Pad #	X (µm)	Y (µm)														
XIN	1	125.00	665.21	I	Crystal input pad												
OE, PDB, FSEL, CLK1	2	85.00	375.00	B	This programmable I/O pin can be configured as an Output Enable (OE) input, Power Down input (PDB), Frequency Select (FSEL) input or CLK1 clock output.												
					<table border="1"> <thead> <tr> <th>State</th> <th>OE</th> <th>PDB</th> <th>FSEL</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Tri-state CLK0</td> <td>Power Down Mode Tri-state CLK0</td> <td>Bank 0</td> </tr> <tr> <td>1 (default)</td> <td>Operating mode</td> <td>Operating mode</td> <td>Bank 1</td> </tr> </tbody> </table>	State	OE	PDB	FSEL	0	Tri-state CLK0	Power Down Mode Tri-state CLK0	Bank 0	1 (default)	Operating mode	Operating mode	Bank 1
					State	OE	PDB	FSEL									
0	Tri-state CLK0	Power Down Mode Tri-state CLK0	Bank 0														
1 (default)	Operating mode	Operating mode	Bank 1														
GND	3	85.00	115.45	P	GND connection												
CLK	4	765.00	115.45	O	Programmable Clock Output												
VDD	5	765.00	375.00	P	VDD connection												
XOUT	6	725.00	665.21	O	Crystal Output pad												

* Note: The X/Y coordinates indicate pad centers.

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PAD ASSIGNMENT AND DESCRIPTION (PL611s-03)

Name	Pad Assignment*			Type	Description												
	Pad #	X (µm)	Y (µm)														
XOUT	1	125.00	665.21	O	Crystal Output pad												
VDD	2	85.00	375.00	P	VDD connection												
CLK	3	85.00	115.45	O	Programmable Clock Output												
GND	4	765.00	115.45	P	GND connection												
OE, PDB, FSEL, CLK1	5	765.00	375.00	B	This programmable I/O pin can be configured as an Output Enable (OE) input, Power Down input (PDB), Frequency Select (FSEL) input or CLK1 clock output.												
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0	Tri-state CLK0	Power Down Mode Tri-state CLK0	Bank 0														
1 (default)	Operating mode	Operating mode	Bank 1														
XIN	6	725.00	665.21	I	Crystal input pad												

* Note: The X/Y coordinates indicate pad centers.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage Range	V _{DD}	-0.5	7	V
Input Voltage Range	V _I	-0.5	V _{DD} +0.5	V
Output Voltage Range	V _O	-0.5	V _{DD} +0.5	V
Data Retention @ 85°C		10		Year
Storage Temperature	T _s	-65	150	°C
Ambient Operating Temperature		-40	85	°C

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

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AC SPECIFICATIONS

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Input Frequency (XIN)	Fundamental Crystal	10		50	MHz
Output Frequency	@ $V_{DD} = 3.3V$			200	MHz
	@ $V_{DD} = 2.5V$			166	
	@ $V_{DD} = 1.8V$			110	
Settling Time	At power-up (after $V_{DD} \geq 1.62V$)			2	ms
Output Enable Time (See MTC-1)	OE Function; $T_a=25^\circ C$, 15pF Load. Add one clock period to this measurement for a usable clock output.			10	ns
	PDB Function; $T_a=25^\circ C$, 15pF Load			2	ms
Output Disable Time (See MTC-1)	$T_a=25^\circ C$, 15pF Load			100	ns
VDD Sensitivity	Frequency vs. $V_{DD} \pm 10\%$	-2		2	ppm
Output Rise Time (See MTC-1)	15pF Load, 10/90% V_{DD} , High Drive, 3.3V, $T_a=25^\circ C$		1	1.5	ns
Output Fall Time (See MTC-1)	15pF Load, 90/10% V_{DD} , High Drive, 3.3V, $T_a=25^\circ C$		1	1.5	ns
Duty Cycle (See MTC-1)	@ 2.5V and 3.3V over entire frequency range, $V_{DD}/2$	45	50	55	%
	@ 1.8V, $\leq 75MHz F_{OUT}$, $V_{DD}/2$	45	50	55	
	@ 1.8V, $75MHz < F_{OUT} \leq 110MHz$	40		60	
Period Jitter, Pk-to-Pk* (10,000 samples measured) (See MTC-3)	With capacitive decoupling between V_{DD} and GND.		70		ps

* Note: Jitter performance depends on the programming parameters.

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DC SPECIFICATIONS

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic, Loaded Output	I_{DD}	@ $V_{DD} = 3.3V$, 30MHz, load=15pF		6.0		mA
Supply Current, Dynamic, Loaded Output	I_{DD}	@ $V_{DD} = 2.5V$, 30MHz, load=15pF		3.9		mA
Supply Current, Dynamic, Loaded Output	I_{DD}	@ $V_{DD} = 1.8V$, 30MHz, load=5pF		2.1		mA
PLL Off: Supply Current, Dynamic, Loaded Output	I_{DD}	@ $V_{DD} = 3.3V$, 30MHz, load=15pF		2.0		mA
PLL Off: Supply Current, Dynamic, Loaded Output	I_{DD}	@ $V_{DD} = 2.5V$, 30MHz, load=15pF		1.6		mA
PLL Off: Supply Current, Dynamic, Loaded Output	I_{DD}	@ $V_{DD} = 1.8V$, 30MHz, load=5pF		0.8		mA
Stand By Current, Loaded Outputs (See MTC-1)	I_{DD}	When PDB=0			<10	μA
Operating Voltage	V_{DD}		1.62		3.63	V
Output Low Voltage	V_{OL}	$I_{OL} = +4mA$ Standard Drive			0.4	V
Output High Voltage	V_{OH}	$I_{OH} = -4mA$ Standard Drive	$V_{DD} - 0.4$			V
Output Current, Low Drive (See MCT-2)	I_{OSD}	$V_{OL} = 0.4V$, $V_{OH} = 2.4V$, 3.3V Operation	4			mA
Output Current, Standard Drive (See MCT-2)	I_{OSD}	$V_{OL} = 0.4V$, $V_{OH} = 2.4V$, 3.3V Operation	8			mA
Output Current, High Drive (See MCT-2)	I_{OHD}	$V_{OL} = 0.4V$, $V_{OH} = 2.4V$, 3.3V Operation	16			mA

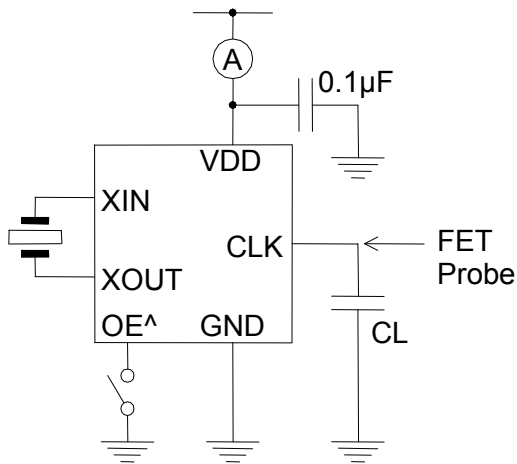
CRYSTAL SPECIFICATIONS

PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNITS
Fundamental Crystal Resonator Frequency	F_{XIN}	10		50	MHz
Crystal Loading Rating (The IC can be programmed for any value in this range.)	$C_{L(xtal)}$	8		12	pF
Maximum Sustainable Drive Level				100	μW
Operating Drive Level			30		μW
Crystal Shunt Capacitance	C_0			4	pF
Effective Series Resistance, Fundamental, 10 - 50MHz (See MCT-4)	ESR			30	Ω

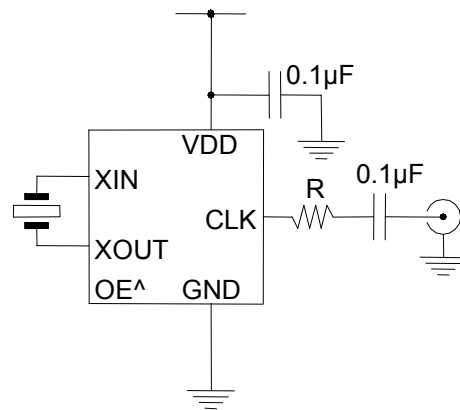
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MEASUREMENT TEST CIRCUITS (MTC)

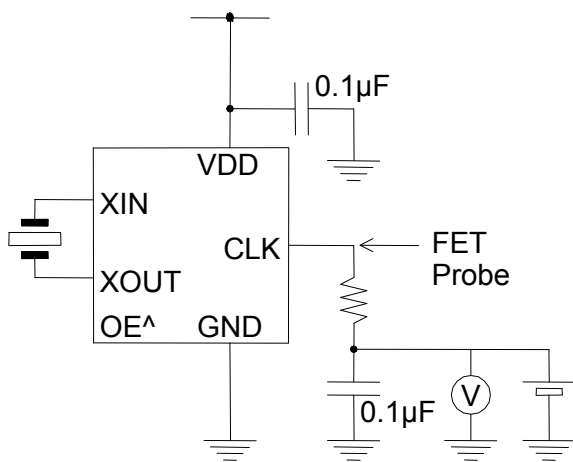
MTC-1: Rise Time, Fall Time, Duty Cycle, VOL, VOH, I_{dd}, Power Down Current, Output Enable/Disable



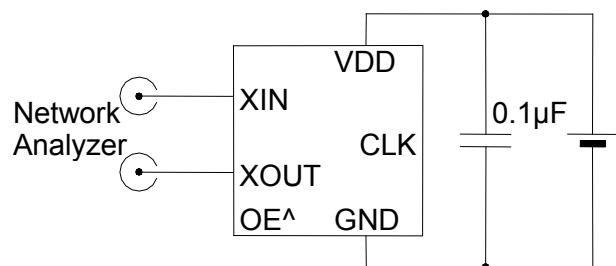
MTC-3: Jitter and Phase Noise



MTC-2: Output Drive Current and Output Impedance



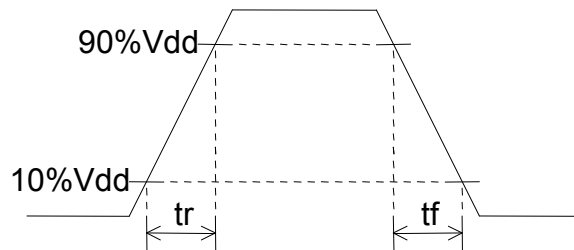
MTC-4: Negative Resistance



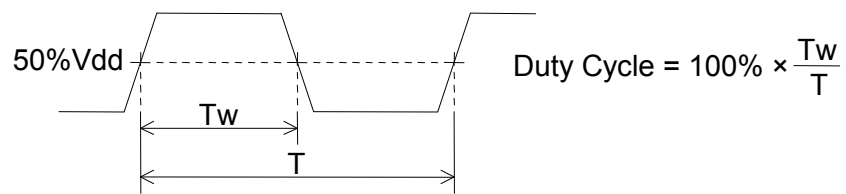
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WAVEFORM SWITCHING CHARACTERISTICS

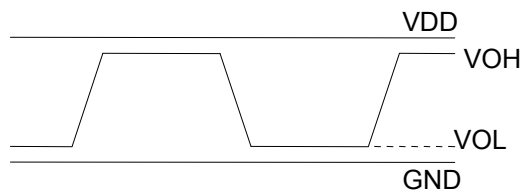
Rise and Fall times:



Duty Cycle:



VOH, VOL:



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ORDERING INFORMATION

For part ordering, please contact our Sales Department:

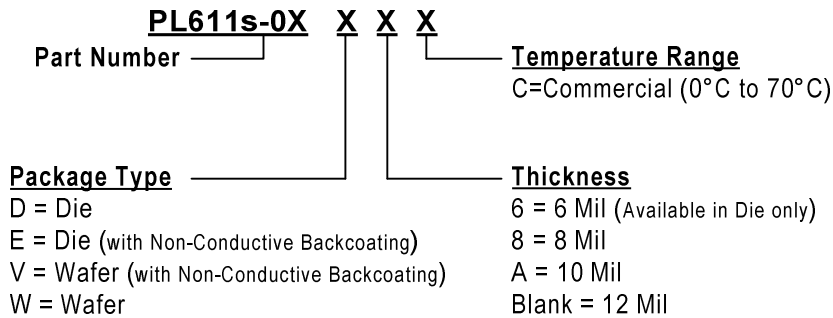
47745 Fremont Blvd., Fremont, CA 94538, USA

Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:

Part number, Package type and Operating temperature range



Part / Order Number	Package Option	Temperature
PL611s-02DxC	Die (Waffle Pack)	0°C to +70°C
PL611s-02ExC	Die (Waffle Pack)	0°C to +70°C
PL611s-02VxC	Wafer	0°C to +70°C
PL611s-02WxC	Wafer	0°C to +70°C
PL611s-03DxC	Die (Waffle Pack)	0°C to +70°C
PL611s-03ExC	Die (Waffle Pack)	0°C to +70°C
PL611s-03VxC	Wafer	0°C to +70°C
PL611s-03WxC	Wafer	0°C to +70°C

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