1.8V-3.3V PicoPLL™ Programmable Clock

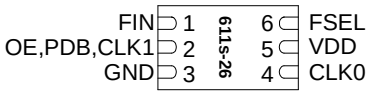
FEATURES

- Advanced One Time Programmable (OTP) PLL design
- Programmable PLL or direct oscillation operation
- Very low Jitter and Phase Noise (30-70ps Pk-Pk typ.)
- Output Frequency up to
  - o 110MHz @ 1.8V operation
  - o 166MHz @ 2.5V operation
  - o 200MHz @ 3.3V operation
- DC Coupled Reference Input Frequency
  - o 1MHz to 200MHz
- Low current consumption, <50µA when PDB is activated
- One programmable I/O pin can be configured as Output Enable (OE),Power Down (PDB) input or an additional clock output (CLK1).
- Dedicated Frequency Switching (FSEL) capability
- Single 1.8V ~ 3.3V, ± 10% power supply
- Operating temperature range from -40°C to 85°C
- Available in 6-pin DFN and SOT23 GREEN/RoHS compliant packages.

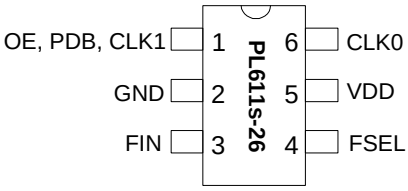
DESCRIPTION

The PL611s-26 is a general purpose frequency synthesizer and a member of PhaseLink's PicoPLL™ product family. Designed to fit in a small 6-pin DFN or 6-pin SOT package for high performance applications, the PL611s-26 offers very low phase noise, jitter, and power consumption, while offering up to 2 clock outputs.. The Frequency Switching (FSEL) capability of PL611s-26 allows for programming two sets of frequencies, while the power down feature of PL611s-26, when activated, allows the IC to consume less than 50µA of power. PL611s-26's programming flexibility allows generating any output using Reference input signal.

PACKAGE PIN CONFIGURATION AND DESCRIPTION

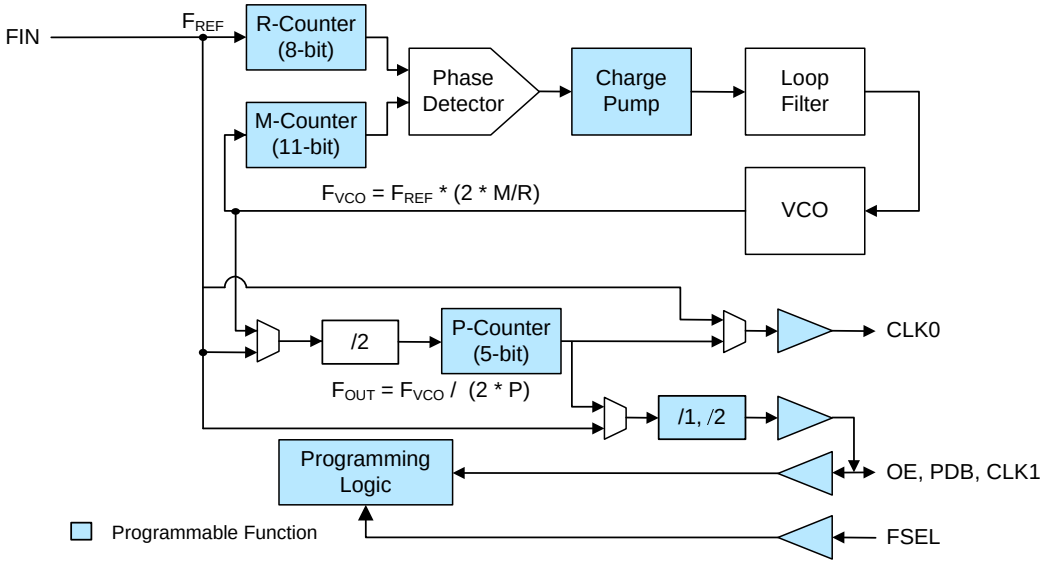


DFN-6L
(2.0 x 1.3 x 0.6mm)



SOT23-6L
(3.0 x 3.0 x 1.35mm)

BLOCK DIAGRAM



KEY PROGRAMMING PARAMETERS

CLK Output Frequency	Output Drive Strength	Programmable Input/Output
$F_{OUT} = F_{REF} * M / (R * P)$ Where M = 11 bit R = 8 bit P = 5 bit CLK0 = F_{OUT}, F_{REF} or $F_{REF} / (2*P)$ CLK1 = F_{REF}, $F_{REF}/2$, CLK0 or CLK0/2	Three optional drive strengths to choose from: • Low: 4mA • Std: 8mA (default) • High: 16mA	One output pin can be configured as: • OE - input • PDB - input • CLK1 – output

PIN DESCRIPTION

Name	Pin Assignment		Type	Description
	DFN Pin#	SOT Pin #		
OE, PDB, CLK1	2	1	I/O	This programmable I/O pin can be configured as an Output Enable (OE) input, Power Down input (PDB) or CLK1 Clock output. This pin has an internal 60KΩ pull up resistor (OE and PDB functions only).
GND	3	2	P	GND connection
FIN	1	3	I	Reference input pin
FSEL	6	4	I	Frequency Switching Input pin. This pin has an internal 60KΩ pull up resistor.
VDD	5	5	P	VDD connection
CLK0	4	6	O	Programmable Clock Output

Pin State	OE	PDB
0	Disable CLK	Power Down Mode
1 (default)	Normal mode	Normal mode

FSEL	State
0	Frequency 2
1 (default)	Frequency 1

FUNCTIONAL DESCRIPTION

PL611s-26 is a highly featured, very flexible, advanced programmable PLL design for high performance, low-power, small form-factor applications. The PL611s-26 accepts a reference clock input of 1MHz to 200MHz and is capable of producing two outputs up to 200MHz. This flexible design allows the PL611s-26 to deliver any PLL generated frequency, FREF (Ref Clk) frequency or FREF /(2*P) to CLK0 and/or CLK1. Some of the design features of the PL611s-26 are mentioned below:

PLL Programming

The PLL in the PL611s-26 is fully programmable. The PLL is equipped with an 8-bit input frequency divider (R-Counter), and an 11-bit VCO frequency feedback loop divider (M-Counter). The output of the PLL is transferred to a 5-bit post VCO divider (P-Counter). The output frequency is determined by the following formula [FOUT = FREF * M / (R * P)].

Clock Output (CLK0)

CLK0 is the main clock output. The PL611s-26 can also be programmed to provide a second clock output, CLK1, on the programmable I/O pin (see OE/PDB/CLK1 pin description below). The output of CLK0 can be configured as the PLL output (F_{VCO}/(2*P)), FREF (Ref Clk Frequency) output, or FREF/(2*P) output. The output drive level can be programmed to Low Drive (4mA), Standard Drive (8mA) or High Drive (16mA). The maximum output frequency is determined by the power supply voltage as shown below:

Clock Output (CLK1)

The CLK1 feature allows the PL611s-26 to have an additional clock output. This output can be programmed to one of the following:

FREF - Reference (Ref Clk) Frequency
FREF / 2
CLK0
CLK0 / 2

Frequency Select (FSEL)

The Frequency Select (FSEL) feature allows the PL611s-26 to switch between two pre-programmed outputs allowing the device “On the Fly” frequency switching. The FSEL pin incorporates a pull up resistor giving a default condition of logic “1”.

Output Enable (OE)

The Output Enable feature allows the user to enable and disable the clock output(s) by toggling the OE pin. The OE pin incorporates a pull up resistor giving a default condition of logic “1”.

Power-Down Control (PDB)

The Power Down (PDB) feature allows the user to put the PL611s-26 into “Sleep Mode”. When activated (logic ‘0’), PDB ‘Disables the PLL, the oscillator circuitry, counters, and all other active circuitry. In Power Down mode the IC consumes <50µA of power. The PDB pin incorporates a pull up resistor giving a default condition of logic “1”.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage Range	V_{DD}	-0.5	7	V
Input Voltage Range	V_I	-0.5	V_{DD}+0.5	V
Output Voltage Range	V_O	-0.5	V_{DD}+0.5	V
Soldering Temperature (Green package)			260	°C
Data Retention @ 85°C		10		Year
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*		-40	85	°C

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. *Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

AC SPECIFICATIONS

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input (FIN) Frequency	@ V_{DD} =3.3V	1		200	MHz
	@ V_{DD} =2.5V			166	
	@ V_{DD} =1.8V			110	
Input (FIN) Signal Amplitude	Internally DC Coupled, LVCMOS input, High	0.7*V_{DD}			Vpp
	Internally DC Coupled, LVCMOS input, Low			0.3*V_{DD}	
Output Frequency	@ V_{DD} =3.3V			200	MHz
	@ V_{DD} =2.5V			166	MHz
	@ V_{DD} =1.8V			110	MHz
Settling Time	At power-up (after V_{DD} increases over 1.62V)			2	ms
Output Enable Time	OE Function; Ta=25° C, 15pF Load. Add one clock period to this measurement for a usable output.			10	ns
	PDB Function; Ta=25° C, 15pF Load			2	ms
Output Rise Time	15pF Load, 10/90% V_{DD}, High Drive, 3.3V		1.2	1.7	ns
Output Fall Time	15pF Load, 90/10% V_{DD}, High Drive, 3.3V		1.2	1.7	ns
Duty Cycle	@2.5V and 3.3V over entire frequency range, $V_{DD}/2$	45	50	55	%
	@1.8V, ≤ 75MHz F_{OUT}, $V_{DD}/2$	45	50	55	
	@1.8V, 75MHz < F_{OUT} ≤110MHz	40		60	
Period Jitter, Pk-to-Pk* (10,000 samples measured)	With capacitive decoupling between V_{DD} and GND		70		ps

* Note: Jitter performance depends on the programming parameters.

DC SPECIFICATIONS

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic	I_{DD}	V_{DD} =3.3V, 27MHz, load=15pF		5.5		mA
Supply Current, Dynamic	I_{DD}	V_{DD} =2.5V, 27MHz, load=15pF		3.8		mA
Supply Current, Dynamic	I_{DD}	V_{DD} =1.8V, 27MHz, load=15pF		1.8		mA
Stand By Current	I_{DD}	When PDB=0			<50	µA
Operating Voltage	V_{DD}		1.62		3.63	V
Power Supply Ramp	t_{PU}	Time for V_{DD} to reach 90% V_{DD}. Power ramp must be monotonic.			100	ms
Output Low Voltage	V_{OL}	I_{OL} = +4mA Standard Drive			0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4mA Standard Drive	V_{DD} – 0.4			V
Output Current, Low Drive	I_{OSD}	V_{OL} = 0.4V, V_{OH} = 2.4V	4			mA
Output Current, Standard Drive	I_{OSD}	V_{OL} = 0.4V, V_{OH} = 2.4V	8			mA
Output Current, High Drive	I_{OHD}	V_{OL} = 0.4V, V_{OH} = 2.4V	16			mA

LAYOUT RECOMMENDATIONS

The following guidelines are to assist you with a performance optimized PCB design:

Signal Integrity and Termination Considerations

- Keep traces short!

- Trace = Inductor. With a capacitive load this equals ringing!

- Long trace = Transmission Line. Without proper termination this will cause reflections (looks like ringing).

- Design long traces (> 1 inch) as “striplines” or “microstrips” with defined impedance.

- Match trace at one side to avoid reflections bouncing back and forth.

Decoupling and Power Supply Considerations

- Place decoupling capacitors as close as possible to the VDD pin(s) to limit noise from the power supply

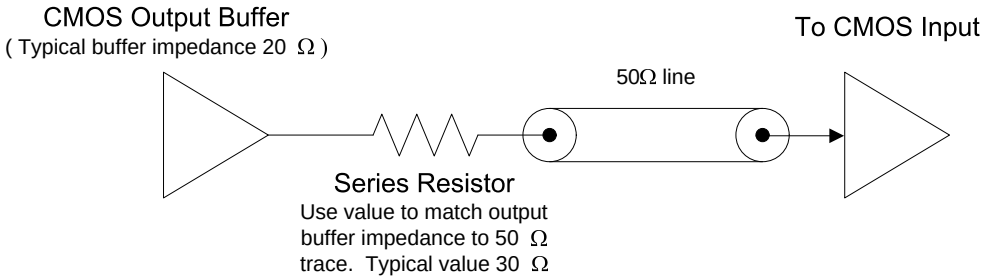
- Multiple VDD pins should be decoupled separately for best performance.

- Addition of a ferrite bead in series with VDD can help prevent noise from other board sources

- Value of decoupling capacitor is frequency dependant. Typical values to use are 0.1μF for designs using frequencies < 50MHz and 0.01μF for designs using frequencies > 50MHz.

Typical CMOS termination

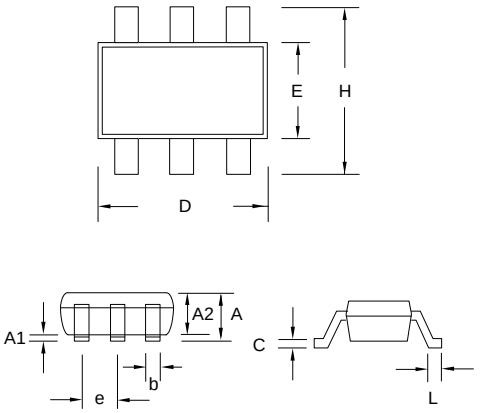
Place Series Resistor as close as possible to CMOS output



PACKAGE DRAWINGS (GREEN PACKAGE COMPLIANT)

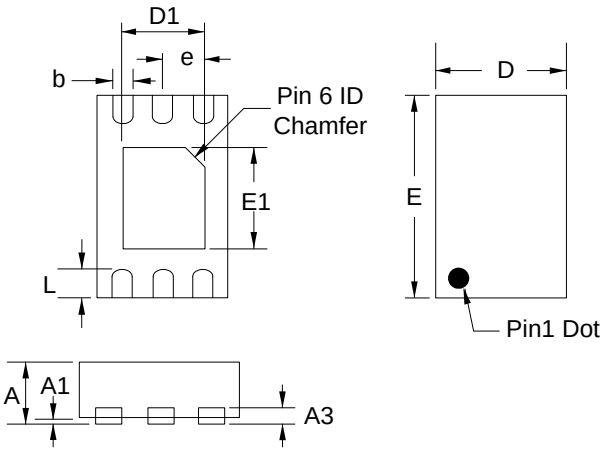
SOT23-6L

Symbol	Dimension in MM	
	Min.	Max.
A	1.05	1.35
A1	0.05	0.15
A2	1.00	1.20
b	0.30	0.50
c	0.08	0.20
D	2.80	3.00
E	1.50	1.70
H	2.60	3.0
L	0.35	0.55
e	0.95 BSC	



DFN-6L

Symbol	Dimension in MM	
	Min.	Max.
A	0.50	0.60
A1	0.00	0.05
A3	0.152	0.152
b	0.15	0.25
e	0.40BSC	
D	1.25	1.35
E	1.95	2.05
D1	0.75	0.85
E1	0.95	1.05
L	0.20	0.30



ORDERING INFORMATION (GREEN PACKAGE COMPLIANT)

For part ordering, please contact our Sales Department:
47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER
The order number for this device is a combination of the following:
Part number, Package type and Operating temperature range

PL611s-26-XXX X X - X

- **PL611s-26-XXX** — Part Number
- **XXX** — 3 DIGIT ID Code * (will be assigned at programming time)
- **X** — Package Type
  - G=DFN-6L
  - T=SOT23-6L
- **X** — Temperature
  - C=Commercial (0°C to 70°C)
  - I=Industrial (-40°C to 85°C)
- **X** — Shipping Option
  - None=Tube
  - R=Tape & Reel

* PhaseLink will assign a unique 3-digit ID code for each approved programmed part number.

Part/Order Number	Marking†	Package Option
PL611s-26-XXXGC-R	XXX	6-Pin DFN (Tape and Reel)
PL611s-26-XXXTC-R	26XXX	6-Pin SOT23 (Tape and Reel)

† Note: 'XXX' designates marking identifier that, at times, could be independent of the part number. Please consult your PhaseLink sales representative for marking information.

Solder reflow profile available at www.phaselink.com/QA/solderingGreen.pdf