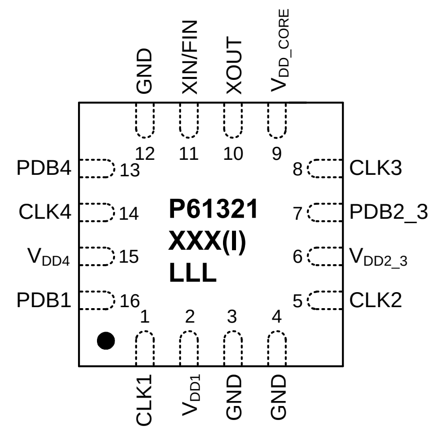
Ultra Low Power PicoPLL, Programmable 3-PLL Clock IC

FEATURES

- Designed for PCB Space Savings with 3 Low-Power Programmable PLLs
- Ultra Low-Power Consumption
- Ultra-Low Power Down Mode, <5µA Typical
- CLK1 Capable of Generating 32.768kHz
- Individual Output Buffer V_{DD} Pins for Flexible Output Voltages, 1.8V to 3.3V, ±10%
- Individual PLL Power Down Control
- Output Frequency (based on V_{DD_CORE} voltage):
  - o ≤65MHz @ 1.8V operation
  - o ≤90MHz @ 2.5V operation
  - o ≤125MHz @ 3.3V operation
- Input Frequency:
  - o Fundamental Crystal: 10MHz to 40MHz
  - o Reference Input: 10MHz to 200MHz
- Active Low or Hi-Z Disabled Output State
- 1.8V to 3.3V, ±10% Core Power Supply
- 1.8V to 3.3V, ±10% Buffer Power Supply
- Operating Temperature Ranges:
  - o Commercial: 0°C to 70°C
  - o Industrial: -40°C to 85°C
- Available in GREEN/RoHS Compliant 3x3 QFN Package

PIN CONFIGURATION



QFN-16L Package

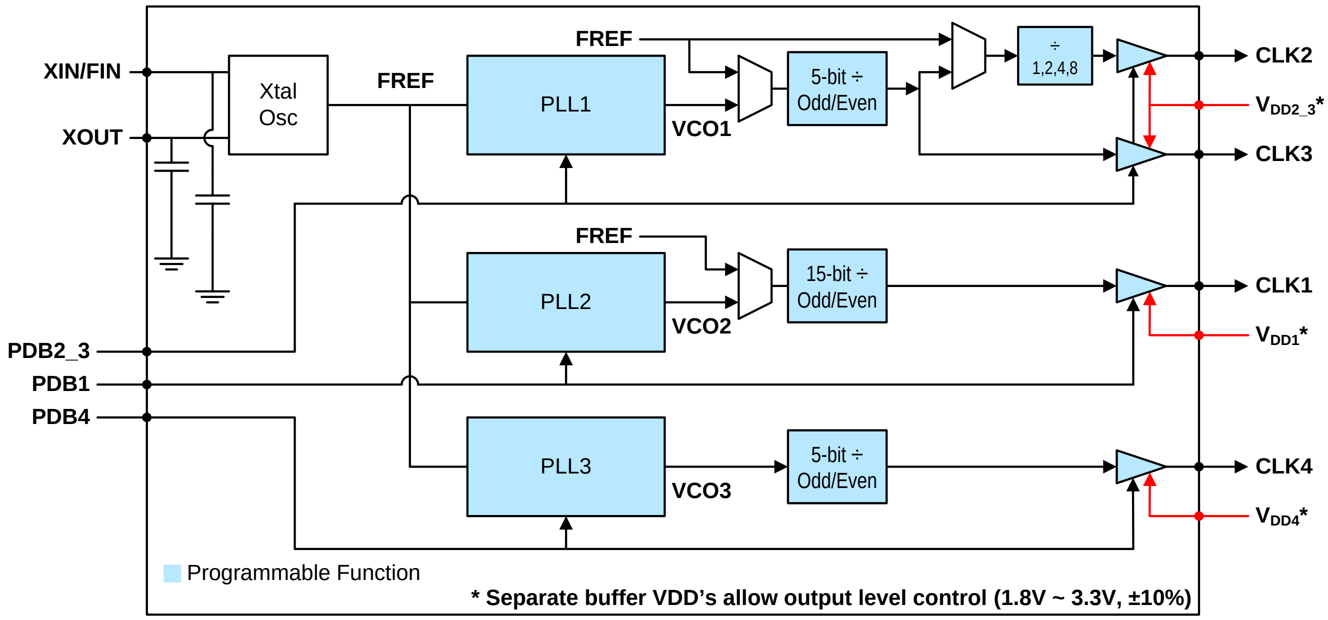
DESCRIPTION

The PL613-21 is an advanced three PLL design based on PhaseLink's PicoPLL, the world's smallest programmable clock technology. This advanced technology allows the PL613-21 to fit in to a small 3x3mm QFN package for high performance, low-power, small form-factor applications. By using the individual output buffer V_{DD} pins, the PL613-21 can support multiple output voltage requirements. In addition, CLK1 has the ability to generate kHz outputs and is ideal for generating 32.768kHz outputs.

The unique power down features of the PL613-21 allows the user to shut down individual PLLs when the corresponding clock output is disabled using the PDB pins. The output drive strength can be individually programmed on each output to Low (4mA), Standard (8mA) or High (16mA) drive. In addition, the disabled state of the clock outputs can be programmed as Hi-Z or Active Low.

Besides its small form factor and multiple outputs that can reduce overall system costs, the PL613-21 offers superior phase noise, jitter and power consumption performance.

BLOCK DIAGRAM



PACKAGE PIN ASSIGNMENT

Name	Package Pin # QFN-16L	Type	Description
CLK1	1	I	Programmable clock output
V_{DD1}	2	P	V_{DD} connection for output buffer CLK1
GND	3, 4, 12	P	GND connection
CLK2	5	O	Programmable clock output
V_{DD2_3}	6	P	V_{DD} connection for output buffers CLK2 and CLK3
PDB2_3*	7	I	Power down input for PLL1, CLK2 and CLK3
CLK3	8	O	Programmable clock output
V_{DD_CORE}	9	P	V_{DD} connection for core
XOUT	10	O	Crystal output pin. Do Not Connect when using FIN
XIN/FIN	11	I	Crystal or Reference Clock input
PDB4*	13	I	Power down input for PLL3 and CLK4
CLK4	14	O	Programmable clock output
V_{DD4}	15	P	V_{DD} connection for output buffer CLK4
PDB1*	16	I	Power down input for PLL2 and CLK1

*Note: The PDB pins have no internal pull up or pull down resistors. These pins must be driven to a logic 1 (≥1.62V) or logic 0 (≤ 0.4V) at startup to stabilize the corresponding output(s).

POWER DOWN OPERATION

The PL613-21 has three pins which allow the user to power down each PLL and its corresponding clock output(s) when not in use. When all three PDB pins are pulled low the device enters full power down mode and draws <5µA typical. The disabled state of the clock outputs can be programmed as Hi-Z or Active Low.

PDB INPUT			INTERNAL BLOCK				OUTPUT			
PDB1	PDB2_3	PDB4	Oscillator	PLL1	PLL2	PLL3	CLK1	CLK2	CLK3	CLK4
1	1	1	running	running	running	running	ON	ON	ON	ON
1	1	0	running	running	running	power down	ON	ON	ON	OFF
1	0	1	running	power down	running	running	ON	OFF	OFF	ON
1	0	0	running	power down	running	power down	ON	OFF	OFF	OFF
0	1	1	running	running	power down	running	OFF	ON	ON	ON
0	1	0	running	running	power down	power down	OFF	ON	ON	OFF
0	0	1	running	power down	power down	running	OFF	OFF	OFF	ON
0	0	0	power down	power down	power down	power down	OFF	OFF	OFF	OFF

Note: Typical output enable time is <100µs for single PDB operation when any other PDB pin is high. When part is in full power down mode (all three PDB pins in low state) the typical output enable time is <2mS.

The PDB pins have no internal pull up or pull down resistors. These pins must be driven to a logic 1 (≥1.62V) or logic 0 (≤0.4V) at startup to stabilize the corresponding output(s).

If the output from CLK1 and/or CLK4 will not be used in a design then the corresponding PDB pin must be tied to GND.

Power up in Power Down

The PDB pins should be grounded or connected to the corresponding V_{DD}s during power-up. If the PDB pins are grounded during power up the power down current is not guaranteed immediately after power-up. The Power Down current will be in spec if at least one PDB pin is pulled high for at least 2mS after power-up and then pulled low.

CORE AND BUFFER POWER SUPPLIES

The PL613-21 is capable of supporting multiple voltage levels for the core and buffers. The core voltage is supplied at pin 9 (V_{DD_CORE}) and can operate at a nominal V_{DD_CORE} between 1.8V and 3.3V. The tolerance of V_{DD_CORE} is ±10%.

There are three output buffer voltage inputs which allow multiple output voltages to be supported by one device.

Pin	CLK Buffer	Operating Voltage
V_{DD1} (Pin 2)	CLK1	1.8V to 3.3V, ±10%
V_{DD2_3} (Pin 6)	CLK2 CLK3	1.8V to 3.3V, ±10%
V_{DD4} (Pin 15) (See VDD_CORE vs. VDD4 Design Considerations and Requirements below)	CLK4	1.8V to 3.3V, ±10%

This flexible power supply structure allows the core device to run at the lowest available V_{DD} and still support higher V_{DD} swing outputs.

V_{DD_CORE} VS. V_{DD4} DESIGN CONSIDERATIONS AND REQUIREMENTS

1. Power supply voltage (DC) at V_{DD4} must be greater than or equal to power supply voltage (DC) at V_{DD_CORE} ($V_{DD4} \geq V_{DD\_CORE}$).
2. If V_{DD4} and V_{DD_CORE} are connected to different power supplies, and V_{DD4}=3.3V (±10%), the power supply ramp of V_{DD_CORE} power supply must come before the power supply ramp of V_{DD4} power supply.

The ramp time of V_{DD_CORE} and V_{DD4} must be from 100µS to 250mS. They must be monotonic.

LAYOUT RECOMMENDATIONS

The following guidelines are to assist you with a performance optimized PCB design:

Signal Integrity and Termination Considerations

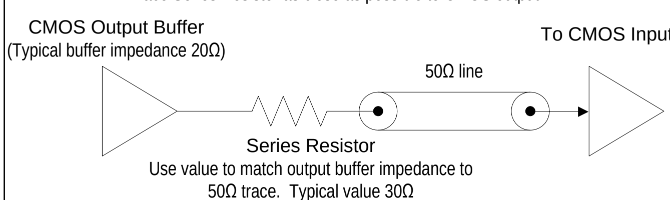
- Keep traces short!
- Trace = Inductor. With a capacitive load this equals ringing!
- Long trace = Transmission Line. Without proper termination this will cause reflections (looks like ringing).
- Design long traces (<1 inch) as “striplines” or “microstrips” with defined impedance.
- Match trace at one side to avoid reflections bouncing back and forth.

Decoupling and Power Supply Considerations

- Place decoupling capacitors as close as possible to the V_{DD} pin(s) to limit noise from the power supply
- Multiple V_{DD} pins should be decoupled separately for best performance.
- Addition of a ferrite bead in series with V_{DD} can help prevent noise from other board sources
- Value of decoupling capacitor is frequency dependant. Typical values to use are 0.1µF for designs using frequencies < 50MHz and 0.01µF for designs using frequencies > 50MHz.

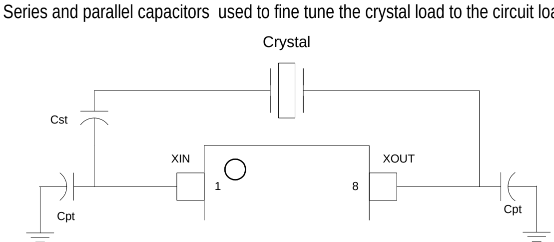
Typical CMOS termination

Place Series Resistor as close as possible to CMOS output



Crystal Tuning Circuit

Series and parallel capacitors used to fine tune the crystal load to the circuit load.



CST – Series Capacitor, used to lower circuit load to match crystal load. Raises frequency offset. This can be eliminated by using a crystal with a Cload of equal or greater value than the oscillator. CPT – Parallel Capacitors, Used to raise the circuit load to match the crystal load. Lowers frequency offset.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	SYMBOL	MIN	MAX	UNITS
Supply Voltage Range	V_{DD}	-0.5	4.6	V
Input Voltage Range	V_I	-0.5	V_{DD}+0.5	V
Output Voltage Range	V_O	-0.5	V_{DD}+0.5	V
Soldering Temperature			260	°C
Data Retention @ 85°C		10		Year
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature		-40	85	°C

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

DC SPECIFICATIONS

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current, All V_{DD} = 3.3V	I_{DD}	Input 16.368MHz fundamental mode crystal, CLK2,3,4 outputs at 40MHz, CLK1 output at 32.768kHz, No Load.		9.2		mA
Supply Current, All V_{DD} = 2.5V	I_{DD}			6.5		mA
Supply Current, All V_{DD} = 1.8V	I_{DD}			4.7		mA
Supply Current	I_{DD}	When all PDB=0, 25°C		5		µA
Typical V_{DD_CORE} Operating Voltages	V_{DD_CORE}	3.3V Operation	2.97	3.3	3.63	V
		2.5V Operation	2.25	2.5	2.75	
		1.8V Operation	1.62	1.8	1.98	
Power Supply Ramp	t_{PU}	Time for V_{DD_CORE} and V_{DD4} to reach 90% target V_{DD}. Power ramp must be monotonic.	0.5		250	ms
V_{DDx} Buffer Voltage	V_{DDx}		1.62		3.63	V
Output Low Voltage	V_{OL}	I_{OL} = +4mA, V_{DDX} = 3.3V			0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4mA, V_{DDX} = 3.3V	2.4			V
Output Current, Low Drive	I_{OLD}	V_{OL} = 0.4V, V_{OH} = 2.4V, V_{DD}=3.3V	±4			mA
Output Current, Std Drive	I_{OSD}	V_{OL} = 0.4V, V_{OH} = 2.4V, V_{DD}=3.3V	±8			mA
Output Current, High Drive	I_{OHD}	V_{OL} = 0.4V, V_{OH} = 2.4V, V_{DD}=3.3V	±16			mA

AC SPECIFICATIONS

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Input (XIN) Frequency	Fundamental Crystal	10		40	MHz
Input (FIN) Frequency	$V_{DD\_CORE} \geq 2.5V$	10		200	MHz
	$V_{DD\_CORE} = 1.8V$	10		100	
Input (FIN) Signal Amplitude	Internally AC coupled (High Frequency)	0.8		3.3	V_{PP}
Output Frequency CLK2, CLK3, CLK4	$V_{DDx} = 3.3V$	1		125	MHz
	$V_{DDx} = 2.5V$			90	
	$V_{DDx} = 1.8V$			65	
Output Frequency CLK1	$V_{DD1} = 3.3V$	0.0002		13	MHz
	$V_{DD1} = 2.5V$			13	
	$V_{DD1} = 1.8V$			1	
Settling Time	At power-up (after V_{DD_CORE} & V_{DD4} >90% V_{DD})		2	5	ms
Output Enable Time	PDBx Function, In operating mode (at least one other PDB=1); Ta=25ºC, 15pF Load. Add one clock period to this measurement for a usable clock output.			100	µs
	PDBx Function, from full power down (all PDB=0); Ta=25ºC, 15pF Load, F_{IN} or crystal present and > 10MHz		2		ms
VDD Sensitivity	Frequency vs. V_{DD} ±10%	-2		2	ppm
Output Rise Time	15pF Load, 10/90% V_{DD}, High Drive, 3.3V		1.2	1.7	ns
	15pF Load, 10/90% V_{DD}, Std Drive, 3.3V		2.0	3.0	
	15pF Load, 10/90% V_{DD}, Low Drive, 3.3V		6.0	8.0	
Output Fall Time	15pF Load, 90/10% V_{DD}, High Drive, 3.3V		1.2	1.7	ns
	15pF Load, 90/10% V_{DD}, Std Drive, 3.3V		2.0	3.0	
	15pF Load, 90/10% V_{DD}, Low Drive, 3.3V		6.0	8.0	
Duty Cycle for CLK2, CLK3 & CLK4	PLL Enabled, @ V_{DD} /2, Entire Frequency Range, High Drive	45	50	55	%
Duty Cycle for CLK1	PLL Enabled, V_{DD} /2, CLK1 $\leq$ 1MHz	45	50	55	%
	PLL Enabled, V_{DD} /2, 1MHz $\leq$ CLK1 $\leq$ 13MHz (See Output Frequency CLK1)	40	50	60	
Period Jitter, Pk-to-Pk* (10,000 samples)	Configuration Dependent, Outputs $\geq$ 10MHz		300		ps

*: Jitter performance depends on programming parameters

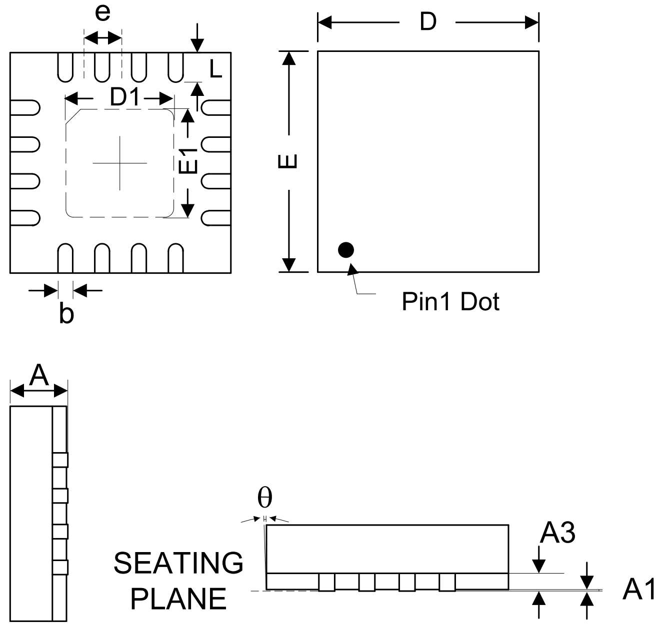
CRYSTAL SPECIFICATIONS

PARAMETERS		SYMBOL	MIN	TYP	MAX	UNITS
Fundamental Crystal Resonator Frequency		F_{XIN}	10		40	MHz
Crystal Loading Rating		$C_{L\ (xtal)}$		15		pF
Operating Drive Level				0.1	2	mW
Metal Can Crystal	Shunt Capacitance	C0			5.5	pF
	ESR Max	ESR			40	Ω
Small SMD Crystal	Shunt Capacitance	C0			2.5	pF
	ESR Max	ESR			60	Ω

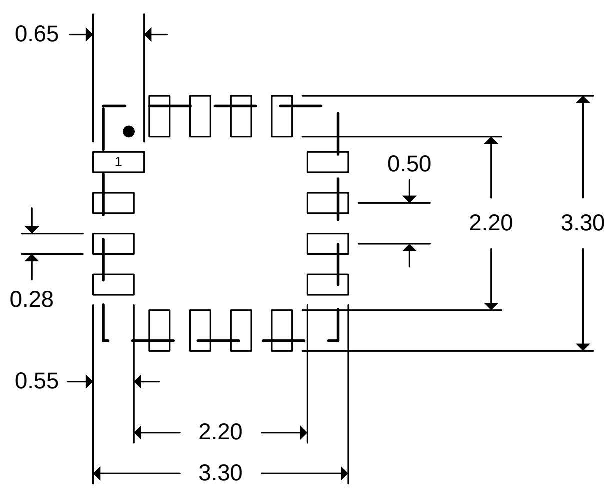
PACKAGE DRAWING (GREEN PACKAGE COMPLIANT)

QFN-16L

Symbol	Dimension (mm)		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.203 Ref		
b	0.20	0.25	0.30
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D1	1.65	1.70	1.75
E1	1.65	1.70	1.75
L	0.250	0.300	0.350
e	0.50BSC		



Recommended Land Pattern (mm)



Note: The pad underneath the QFN package is connected to the substrate. There should be no bare traces or bare metal under the package.

ORDERING INFORMATION (GREEN PACKAGE COMPLIANT)

For part ordering, please contact our Sales Department:
47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER
The order number for this device is a combination of the following:
Part number, Package type and Operating temperature range

PL613-21-XXX Q X R

PART NUMBER

3 DIGIT ID Code * (will be assigned at programming time)

PACKAGE TYPE
Q=QFN-16L

R=TAPE and REEL

TEMPERATURE
C=COMMERCIAL (0°C to 70°C)
I= INDUSTRIAL (-40°C to 85°C)

* PhaseLink will assign a unique 3-digit ID code for each approved programmed part number.

Part Number/Order Number	Marking†	Package Option
PL613-21-XXXQC-R	P61321 XXX(I) LLL	16-Pin QFN (Tape and Reel)

† Marking Notes :
1) The "I" after the three digit programming code will be marked for Industrial Temperature grade products only. Commercial grade products will not have a character in this position.
2) LLL represents the production lot number

Solder reflow profile available at www.phaselink.com/QA/solderingGreen.pdf