38MHz to 640MHz Low Phase Noise XO

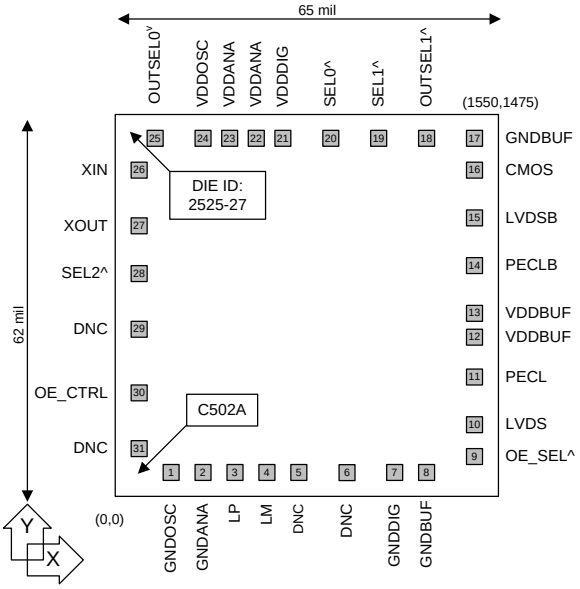
FEATURES

- Less than 0.4ps RMS (12kHz - 20MHz) phase jitter for all frequencies
- Low phase noise output (@ 1MHz offset)
  - o -144dBc/Hz for 106.25MHz
  - o -144dBc/Hz for 156.25MHz
  - o -144dBc/Hz for 212.5MHz
  - o -140dBc/Hz for 312.5MHz
  - o -131dBC/Hz for 622.08MHz
- Fundamental Crystal Input Frequency:
  - o 19MHz to 40MHz (3.3V)
  - o 19MHz to 28.125MHz (2.5V)
- Output Frequency:
  - o 38MHz to 640MHz (3.3V)
  - o 38MHz to 450MHz (2.5V)
- Selectable LVPECL, LVDS, or LVCMOS outputs
- Output Enable selector
- 2.5V to 3.3V operation
- Available in Die form

DESCRIPTION

The PL680-30 is a monolithic low jitter and low phase noise XO, capable of 0.4ps RMS phase jitter and LVPECL, LVDS, or LVCMOS outputs, covering a wide frequency output range up to 640MHz. The PL680-30 is designed to address the demanding requirements of high performance applications such as SONET, GPS, XDSL, etc.

DIE CONFIGURATION

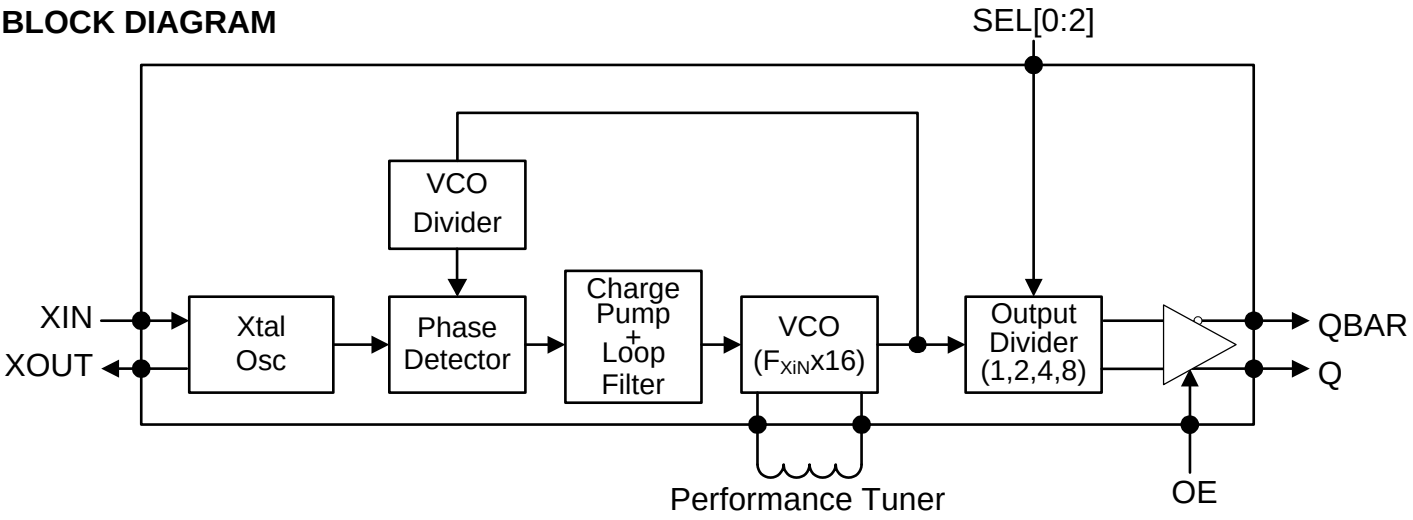


Note1: ^ Denotes internal pull up resistor.

DIE SPECIFICATIONS

Name	Value
Size	62 x 65 mil
Reverse side	GND
Pad dimensions	80 micron x 80 micron
Thickness	10 mil

BLOCK DIAGRAM



OUTPUT ENABLE LOGICAL LEVELS

OUTSEL0ᵛ (Pad #25)	OUTSEL1^ (Pad #18)	Selected Output
0	0	LVDS
0	1	LVPECL (Default)
1	0	High Drive LVCMOS
1	1	Standard Drive LVCMOS

Note: For bonding convenience, 'OUTSEL0' incorporates an internal pull down resistor while 'OUTSEL1' incorporates an internal pull up resistor.

OUTPUT SELECTION AND OUTPUT ENABLE LOGIC

OE_SEL^ (Pad #9)	OE_CTRL (Pad #30)	State
0	0 (Default)	Output enabled
	1	Tri-state
1 (Default)	0	Tri-state
	1 (Default)	Output enabled

Pad #9: Bond to GND to set to "0", bond to VDD or leave floating to set to "1",
Pad #30: Logical states defined by LVPECL levels if OE_SELECT is "0"
Logical states defined by LVCMOS levels if OE_SELECT is "1"

FREQUENCY SELECTION TABLE

SEL2^	SEL1^	SEL0^	Selected Multiplier/Output Frequency
0	0	0	VCO Max*
0	0	1	VCO Min*
0	1	0	Reserved
0	1	1	Reserved
1	0	0	FIN x 2
1	0	1	FIN x 8
1	1	0	FIN x 16
1	1	1	FIN x 4

All SEL pads have 60kΩ internal pull-ups (default value is '1'). Bond to GND to set to "0".
* Special Test Modes to help selecting the inductor value for the target output frequency.

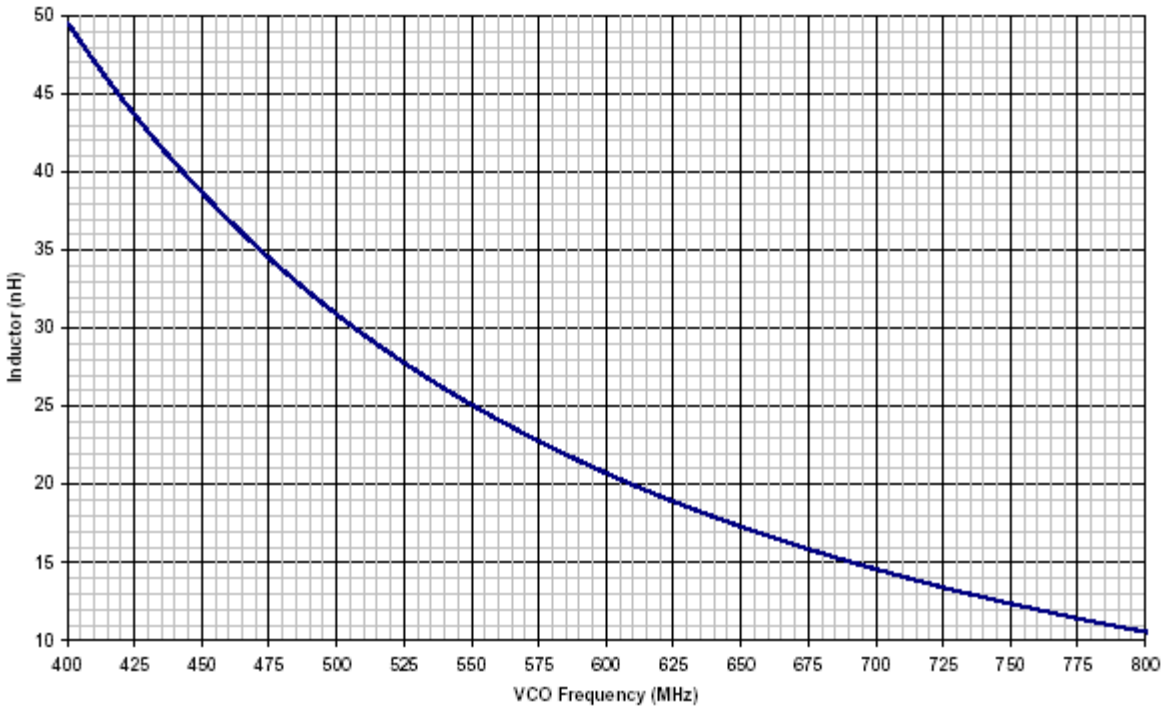
PAD ASSIGNMENT

Pad #	Name	X (μm)	Y (μm)	Description
1	GNDOSC	248	109	Ground, Oscillator circuitry.
2	GNDANA	361	109	Ground, Analog circuitry.
3	LP	473	109	Performance/Frequency tuning Inductor.
4	LM	587	109	Performance/Frequency tuning Inductor.
5	DNC	702	109	Do No Connect.
6	DNC	874	109	Do No Connect.
7	GNDDIG	1042	109	Ground, Digital circuitry.
8	GNDBUF	1171	109	Ground, buffer circuitry.
9	OE_SELECT	1400	125	Used to select between LVPECL or LVCMOS/LVDS logic states for OE. Incorporates a 60kΩ internal pull up resistor.
10	LVDS	1400	259	LVDS Output.
11	PECL	1400	476	LVPECL Output.
12	VDDBUF	1400	616	2.5V ~ 3.3V power supply, Buffer circuitry.
13	VDDBUF	1400	716	2.5V ~ 3.3V power supply, Buffer circuitry.
14	PECLB	1400	871	Complementary LVPECL Output.
15	LVDSB	1400	1089	Complementary LVDS Output.
16	CMOS	1400	1227	Single ended LVCMOS output.
17	GNDBUF	1389	1365	Ground, buffer circuitry.
18	OUTSEL1	1232	1365	Used to select LVCMOS, LVPECL or LVDS output type. Incorporates a 60kΩ internal pull up resistor.
19	SEL1	1042	1365	Used to select multiplication factor. Incorporates a 60kΩ internal pull up resistor.
20	SEL0	854	1365	Used to select multiplication factor. Incorporates a 60kΩ internal pull up resistor.
21	VDDDIG	659	1365	2.5V ~ 3.3V power supply, Digital circuitry.
22	VDDANA	559	1365	2.5V ~ 3.3V power supply, Analog circuitry.
23	VDDANA	459	1365	2.5V ~ 3.3V power supply, Analog circuitry.
24	VDDOSC	358	1365	2.5V ~ 3.3V power supply, Oscillator circuitry.
25	OUTSEL0	194	1365	Used to select CMOS, PECL or LVDS output type. Incorporates a 60kΩ internal pull down resistor.
26	XIN	109	1223	Crystal input. See crystal specification for details.
27	XOUT	109	1017	Crystal output. See crystal specification for details.
28	SEL2	109	858	Used to select multiplication factor. Incorporates internal pull up.
29	DNC	109	646	Do Not Connect
30	OE_CTRL	109	397	Used to enable/disable the output(s). See Output Selection and Output Enable Logic table on page 2. Incorporates a 60kΩ internal pull up (LVCMOS/LVDS) or pull down (LVPECL) resistor.
31	DNC	109	181	Do Not Connect.

PERFORMANCE TUNING & INDUCTOR VALUE SELECTION

Please refer to PhaseLink's 'PhasorV Tuning Assistance' software to automatically calculate the optimum inductor values for your application. In addition, the chart below could be used as a reference for quick inductor value selection. Please note that the inductor values mentioned in the table below, or when using 'PhasorV Tuning Assistance' are derived based on the parasitic values of PhaseLink's evaluation board. For performance enhancement of your custom board design, please follow the following instruction:

Use the special test modes "VCO Max" and "VCO Min" to determine the optimum inductor value. "VCO Max" represents the high end of the VCO range and "VCO Min" represents the low end of the VCO range. The output frequency in the "VCO Max" and "VCO Min" test modes is VCO/16. This means that the output frequencies are around the crystal frequency that will be used. The optimum inductor value is where the target crystal frequency is closest to the middle between the "VCO Max" and "VCO Min" output frequencies. In this case the VCO will lock in the middle of its tuning range with maximum margin on either side.



ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	V_I	-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*	T_A	-40	85	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

* Note: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

2. Crystal Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Resonator Frequency	F_{XIN}	Parallel Fundamental Mode, 3.3V	19		40	MHz
		Parallel Fundamental Mode, 2.5V	19		28.125	
Crystal Loading Rating	$C_{L\ (xtal)}$			18		pF
Crystal Shunt Capacitance	$C_{0\ (xtal)}$				5	pF
Recommended ESR	R_E	AT cut			30	Ω

3. General Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic (Loaded Outputs)	I_{DD}	LVPECL/LVDS /LVCMOS	38MHz<F_{OUT}<100MHz			65/45/30	mA
			100MHz<F_{OUT}<320MHz			80/60/40	
		LVPECL/LVDS	320MHz<F_{OUT}<640MHz			90/70	
Operating Voltage	V_{DD}			2.25**		3.63	V
Output Clock Duty Cycle		@ 50% V_{DD} (LVCMOS) @ 1.25V (LVDS) @ V_{DD} – 1.3V (LVPECL)		45	50	55	%
Short Circuit Current					±50		mA
Stabilization Time *	T_{STB}	From power valid				10	ms

Note: LVCMOS operation is not advised above 200MHz with 15pF load; and 320MHz with 10pF load. Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits. The 2.5V operating supply voltage, denoted by (**), is limited to a maximum output frequency of 450 MHz.

4. Jitter Specifications

PARAMETERS	CONDITIONS	FREQUENCY	MIN.	TYP.	MAX.	UNITS
Integrated jitter RMS	Integrated 12kHz to 20MHz	106.25MHz		0.4	0.5	ps
		156.25MHz		0.4	0.5	
		212.5MHz		0.4	0.5	
		312.5MHz		0.4	0.5	
		622.08MHz		0.4	0.5	
Period jitter RMS	With capacitive decoupling between VDD and GND. Over 10,000 cycles.	106.25MHz		3	5	ps
		156.25MHz		3	5	
		212.5MHz		3	5	
		312.5MHz		3	5	
		622.08MHz		6	8	
Period jitter Peak-to-Peak	With capacitive decoupling between VDD and GND. Over 10,000 cycles.	106.25MHz		20	30	ps
		156.25MHz		20	30	
		212.5MHz		20	30	
		312.5MHz		20	30	
		622.08MHz		40	50	

5. Phase Noise Specifications

PARAMETERS	FREQ.	@10Hz	@100Hz	@1kHz	@10kHz	@100kHz	@1M	@10M	UNITS
Phase Noise relative to carrier (typical)	106.25MHz	-66	-96	-122	-132	-126	-144	-150	dBc/Hz
	156.25MHz	-62	-92	-120	-132	-128	-140	-150	
	212.5MHz	-62	-92	-118	-126	-120	-140	-150	
	312.5MHz	-59	-85	-117	-128	-125	-139	-148	
	622.08MHz	-49	-84	-111	-120	-118	-128	-138	

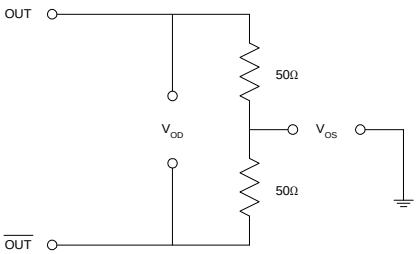
6. LVDS Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Differential Voltage	V_{OD}	R_L = 100Ω (see figure)	247	355	454	mV
V_{DD} Magnitude Change	ΔV_{OD}		-50		50	mV
Output High Voltage	V_{OH}			1.4	1.6	V
Output Low Voltage	V_{OL}		0.9	1.1		V
Offset Voltage	V_{OS}		1.125	1.2	1.375	V
Offset Magnitude Change	ΔV_{OS}		0	3	25	mV
Power-off Leakage	I_{OXD}	V_{out} = V_{DD} or GND, V_{DD} = 0V		±1	±10	uA
Output Short Circuit Current	I_{OSD}			-5.7	-8	mA

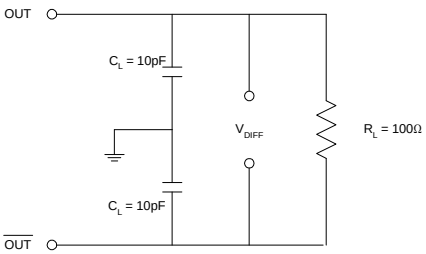
7. LVDS Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Clock Rise Time	t_r	R_L = 100Ω, C_L = 10 pF (see figure)	0.2	0.7	1.0	ns
Differential Clock Fall Time	t_f		0.2	0.7	1.0	ns

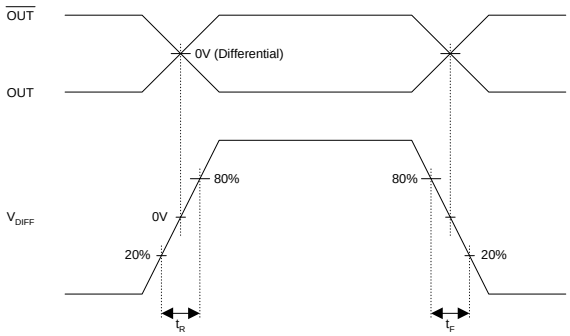
LVDS Levels Test Circuit



LVDS Switching Test Circuit



LVDS Transistion Time Waveform



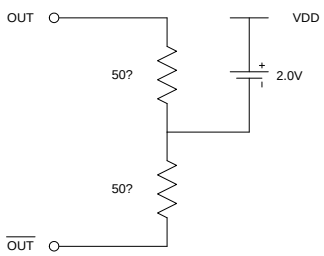
8. LVPECL Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	MAX.	UNITS
Output High Voltage	V_{OH}	R_L = 50Ω to (V_{DD} – 2V) (see figure)	V_{DD} – 1.025		V
Output Low Voltage	V_{OL}			V_{DD} – 1.620	V

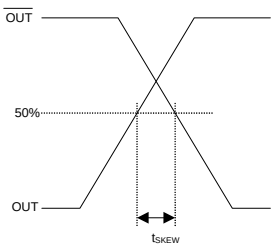
9. LVPECL Switching Characteristics

PARAMETERS	SYMBOL	FREQ.	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Clock Rise & Fall Times	t_r & t_f	<150MHz	@20/80% - LVPECL @80/20% - LVPECL	0.2	0.5	0.7	ns
Clock Rise & Fall Times		>150MHz <320MHz		0.2	0.4	0.55	
Clock Rise & Fall Times		>320MHz		0.2	0.3	0.45	

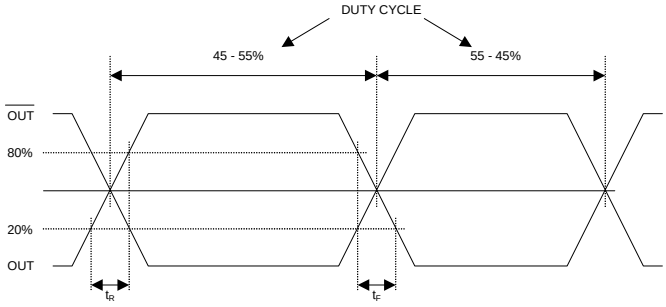
LVPECL Levels Test Circuit



LVPECL Output Skew



LVPECL Transition Time Waveform



11. LVCMOS Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Drive Current Standard Drive	I_{OH}	V_{OH}= V_{DD}-0.4V, V_{DD}=3.3V	10			mA
	I_{OL}	V_{OL} = 0.4V, V_{DD} = 3.3V				
Output Drive Current High Drive	I_{OH}	V_{OH}= V_{DD}-0.4V, V_{DD}=3.3V	30			mA
	I_{OL}	V_{OL} = 0.4V, V_{DD} = 3.3V				
Output Clock Rise/Fall Time Standard Drive	$t_{r/f}$	0.3V ~ 3.0V with 15 pF load		2.5		ns
Output Clock Rise/Fall Time High Drive	$t_{r/f}$	0.3V ~ 3.0V with 15 pF load		1.0		ns

ORDERING INFORMATION

For part ordering, please contact our Sales Department:
47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER
The order number for this device is a combination of the following:
Part number, Package type and Operating temperature range

PL680-30 D C

PART NUMBER

PACKAGE TYPE
D= Die

TEMPERATURE
C=COMMERCIAL (0°C to 70°C)

Part/Order Number	Marking	Package Option
PL680-30DC	P680-30DC	Die (Waffle Pack)