

**Low Phase Noise XO (for HF Fund. and 3<sup>rd</sup> O.T.)**

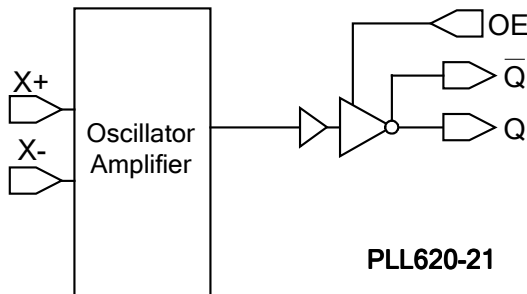
**FEATURES**

- 100MHz to 200MHz Fundamental Mode Crystal.
- Output range: 100 – 200MHz (no multiplication).
- Selectable OE logic.
- Minimum bondwires required for VDD and GND.
- Available outputs: PECL or LVDS.
- Supports 3.3V-Power Supply.
- Available in die form.
- Thickness 10 mil.

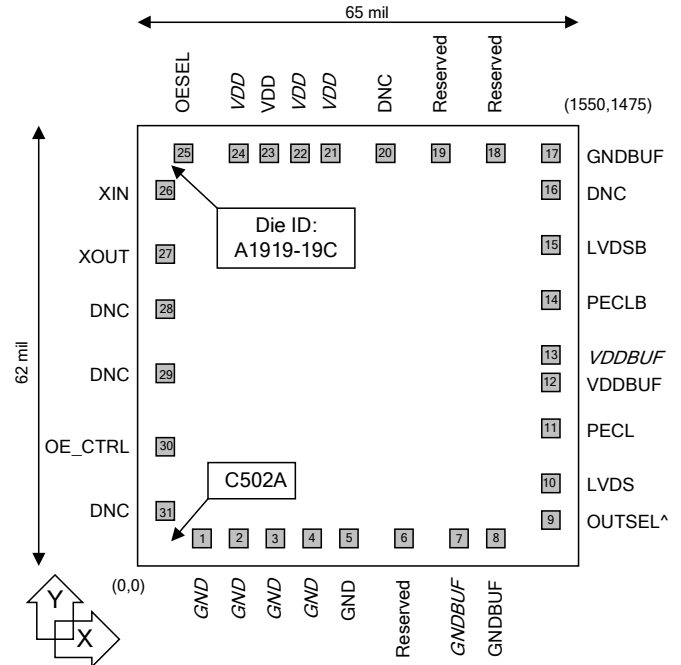
**DESCRIPTIONS**

PLL620-21 is an XO IC specifically designed to work with high frequency fundamental and third overtone crystals. Its design was optimized to tolerate higher limits of interelectrodes capacitance and bonding capacitance to improve yield. It achieves very low current into the crystal resulting in better overall stability. It offers a selectable OE logic and is ideal for XO applications requiring LVDS or PECL output levels at high frequencies.

**BLOCK DIAGRAM**



**DIE CONFIGURATION**



**DIE SPECIFICATIONS**

| Name           | Value                 |
|----------------|-----------------------|
| Size           | 62 x 65 mil           |
| Reverse side   | GND                   |
| Pad dimensions | 80 micron x 80 micron |
| Thickness      | 10 mil                |

**OUTPUT SELECTION AND ENABLE**

| Pad #9<br>OUTSEL | Selected Output |
|------------------|-----------------|
| 0                | LVDS            |
| 1                | PECL (default)  |

| Pad #25<br>OESEL | Pad #30<br>OE_CTRL | State                    |
|------------------|--------------------|--------------------------|
| 0                | 0                  | Tri-state                |
|                  | 1                  | Output enabled (default) |
| 1<br>(default)   | 0                  | Output enabled (default) |
|                  | 1                  | Tri-state                |

Pad #9: Bond to GND to set to "0", bond to VDD to set to "1"  
 Pad #30: Logical states defined by PECL levels if OUTSEL (pad #9) is "1"  
 Logical states defined by CMOS levels if OUTSEL is "0"

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### ELECTRICAL SPECIFICATIONS

#### 1. Absolute Maximum Ratings

| PARAMETERS                                | SYMBOL          | MIN.                 | MAX.                 | UNITS |
|---|-----------------|----------------------|----------------------|-------|
| Supply Voltage                            | V <sub>DD</sub> |                      | 7                    | V     |
| Input Voltage, dc                         | V <sub>I</sub>  | V <sub>SS</sub> -0.5 | V <sub>DD</sub> +0.5 | V     |
| Output Voltage, dc                        | V <sub>O</sub>  | V <sub>SS</sub> -0.5 | V <sub>DD</sub> +0.5 | V     |
| Storage Temperature                       | T <sub>S</sub>  | -65                  | 150                  | °C    |
| Ambient Operating Temperature*            | T <sub>A</sub>  | -40                  | 85                   | °C    |
| Junction Temperature                      | T <sub>J</sub>  |                      | 125                  | °C    |
| Lead Temperature (soldering, 10s)         |                 |                      | 260                  | °C    |
| Input Static Discharge Voltage Protection |                 |                      | 2                    | kV    |

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

\* **Note:** Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for INDUSTRIAL grade only.

#### 2. Crystal Specifications

| PARAMETERS                  | SYMBOL                | CONDITIONS   | MIN. | TYP. | MAX. | UNITS |
|-----------------------------|-----------------------|--|------|------|------|-------|
| Crystal Resonator Frequency | F <sub>XIN</sub>      | Fundamental or 3 <sup>rd</sup> overtone*           | 100  |      | 200  | MHz   |
| Crystal Loading Rating      | C <sub>L (xtal)</sub> | Die only   |      | 3.0  |      | pF    |
| Interelectrode Capacitance  | C <sub>0</sub>        |  |      |      | 3    | pF    |
| Recommended ESR             | R <sub>E</sub>        | F <sub>XIN</sub> <160MHz and C <sub>0</sub> <3.0pF |      |      | 30   | Ω     |
|                             |                       | F <sub>XIN</sub> <200MHz and C <sub>0</sub> <3.0pF |      |      | 25   | Ω     |
|                             |                       | F <sub>XIN</sub> <200MHz and C <sub>0</sub> <2.5pF |      |      | 30   | Ω     |

\* **Note:** 3<sup>rd</sup> overtone crystals require an external resistor between XIN and XOUT to prevent the fundamental from oscillating.

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### 3. General Electrical Specifications

| PARAMETERS                      | SYMBOL          | CONDITIONS  | MIN.     | TYP.     | MAX.     | UNITS |
|---------------------------------|-----------------|---|----------|----------|----------|-------|
| Supply Current (Loaded Outputs) | I <sub>DD</sub> | PECL/LVDS   |          |          | 100/80   | mA    |
| Operating Voltage               | V <sub>DD</sub> |   | 3.13     |          | 3.47     | V     |
| Output Clock Duty Cycle         |                 | @ 1.25V (LVDS)<br>@ V <sub>DD</sub> - 1.3V (PECL) | 45<br>45 | 50<br>50 | 55<br>55 | %     |
| Short Circuit Current           |                 |   |          | ±50      |          | mA    |

### 4. Jitter specifications

| PARAMETERS                                | CONDITIONS   | MIN. | TYP. | MAX. | UNITS |
|---|--|------|------|------|-------|
| Period jitter RMS at 155MHz               | With capacitive decoupling between VDD and GND.                        |      | 2.5  |      | ps    |
| Period jitter peak-to-peak at 155MHz      |  |      | 20   |      |       |
| Accumulated jitter RMS at 155MHz          | With capacitive decoupling between VDD and GND. Over 1,000,000 cycles. |      | 3    |      | ps    |
| Accumulated jitter peak-to-peak at 155MHz |  |      | 25   |      |       |
| Integrated jitter RMS at 155MHz           | Integrated 12 kHz to 20 MHz  |      | 0.3  |      | ps    |

Note: Higher Q factor of 3<sup>rd</sup> overtone crystals will result in even better jitter performance.

### 5. Phase noise specifications

| PARAMETERS                                  | FREQUENCY | @10Hz | @100Hz | @1kHz | @10kHz | @100kHz | UNITS  |
|---|-----------|-------|--------|-------|--------|---------|--------|
| Phase Noise vs. carrier with fund. crystal. | 155.52MHz | -80   | -110   | -125  | -143   | -145    | dBc/Hz |

Note: Higher Q factor of 3<sup>rd</sup> overtone crystals will result in even better phase noise performance.

**Low Phase Noise XO (for HF Fund. and 3<sup>rd</sup> O.T.)**

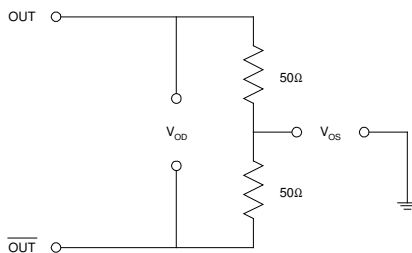
**6. LVDS Electrical Characteristics**

| PARAMETERS                   | SYMBOL          | CONDITIONS                                 | MIN.  | TYP.    | MAX.     | UNITS   |
|------------------------------|-----------------|--|-------|---------|----------|---------|
| Output Differential Voltage  | $V_{OD}$        | $R_L = 100 \Omega$<br>(see figure)         | 247   | 355     | 454      | mV      |
| $V_{DD}$ Magnitude Change    | $\Delta V_{OD}$ |  | -50   |         | 50       | mV      |
| Output High Voltage          | $V_{OH}$        |  |       | 1.4     | 1.6      | V       |
| Output Low Voltage           | $V_{OL}$        |  | 0.9   | 1.1     |          | V       |
| Offset Voltage               | $V_{OS}$        |  | 1.125 | 1.2     | 1.375    | V       |
| Offset Magnitude Change      | $\Delta V_{OS}$ |  | 0     | 3       | 25       | mV      |
| Power-off Leakage            | $I_{OXD}$       | $V_{out} = V_{DD}$ or GND<br>$V_{DD} = 0V$ |       | $\pm 1$ | $\pm 10$ | $\mu A$ |
| Output Short Circuit Current | $I_{OSD}$       |  |       | -5.7    | -8       | mA      |

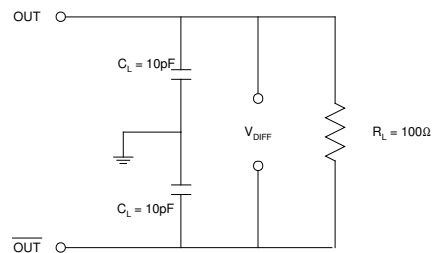
**7. LVDS Switching Characteristics**

| PARAMETERS                   | SYMBOL | CONDITIONS  | MIN. | TYP. | MAX. | UNITS |
|------------------------------|--------|---|------|------|------|-------|
| Differential Clock Rise Time | $t_r$  | $R_L = 100 \Omega$<br>$C_L = 10 \text{ pF}$<br>(see figure) | 0.2  | 0.7  | 1.0  | ns    |
| Differential Clock Fall Time | $t_f$  |   | 0.2  | 0.7  | 1.0  | ns    |

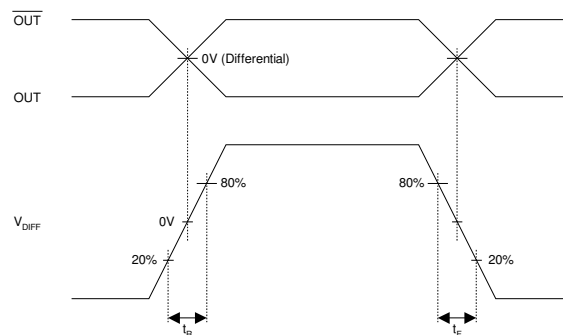
LVDS Levels Test Circuit



LVDS Switching Test Circuit



LVDS Transition Time Waveform



**Low Phase Noise XO (for HF Fund. and 3<sup>rd</sup> O.T.)**

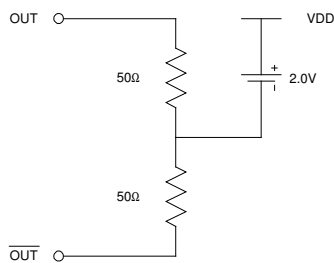
**8. PECL Electrical Characteristics**

| PARAMETERS          | SYMBOL   | CONDITIONS   | MIN.             | MAX.             | UNITS |
|---------------------|----------|--|------------------|------------------|-------|
| Output High Voltage | $V_{OH}$ | $R_L = 50 \Omega$ to $(V_{DD} - 2V)$<br>(see figure) | $V_{DD} - 1.025$ |                  | V     |
| Output Low Voltage  | $V_{OL}$ |  |                  | $V_{DD} - 1.620$ | V     |

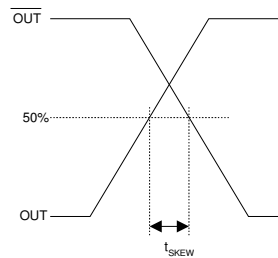
**9. PECL Switching Characteristics**

| PARAMETERS      | SYMBOL | CONDITIONS     | MIN. | TYP. | MAX. | UNITS |
|-----------------|--------|----------------|------|------|------|-------|
| Clock Rise Time | $t_r$  | @20/80% - PECL |      | 0.6  | 1.5  | ns    |
| Clock Fall Time | $t_f$  | @80/20% - PECL |      | 0.5  | 1.5  | ns    |

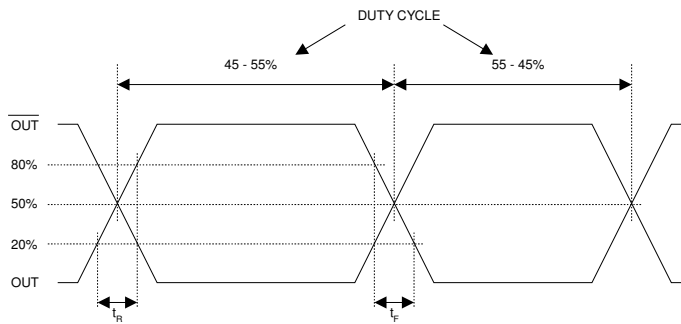
PECL Levels Test Circuit



PECL Output Skew



PECL Transition Time Waveform



## Low Phase Noise XO (for HF Fund. and 3<sup>rd</sup> O.T.)

### PAD ASSIGNMENT

| Pad # | Name                   | X (μm) | Y (μm) |
|-------|------------------------|--------|--------|
| 1     | <i>Optional GND</i>    | 248    | 109    |
| 2     | <i>Optional GND</i>    | 361    | 109    |
| 3     | <i>Optional GND</i>    | 473    | 109    |
| 4     | <i>Optional GND</i>    | 587    | 109    |
| 5     | GND                    | 702    | 109    |
| 6     | <i>Reserved</i>        | 874    | 109    |
| 7     | <i>Optional GNDBUF</i> | 1042   | 109    |
| 8     | GNDBUF                 | 1171   | 109    |
| 9     | OUTSEL                 | 1400   | 125    |
| 10    | LVDS                   | 1400   | 259    |
| 11    | PECL                   | 1400   | 476    |
| 12    | VDDBUF                 | 1400   | 616    |
| 13    | <i>Optional VDDBUF</i> | 1400   | 716    |
| 14    | PECLB                  | 1400   | 871    |
| 15    | LVDSB                  | 1400   | 1089   |
| 16    | <i>Do Not Connect</i>  | 1400   | 1227   |
| 17    | GNDBUF                 | 1389   | 1365   |
| 18    | <i>Reserved</i>        | 1232   | 1365   |
| 19    | <i>Do Not Connect</i>  | 1042   | 1365   |
| 20    | <i>Do Not Connect</i>  | 854    | 1365   |
| 21    | <i>Optional VDD</i>    | 659    | 1365   |
| 22    | <i>Optional VDD</i>    | 559    | 1365   |
| 23    | VDD                    | 459    | 1365   |
| 24    | <i>Optional VDD</i>    | 358    | 1365   |
| 25    | OESEL                  | 194    | 1365   |
| 26    | XIN                    | 109    | 1223   |
| 27    | XOUT                   | 109    | 1017   |
| 28    | <i>Do Not Connect</i>  | 109    | 858    |
| 29    | <i>Do Not Connect</i>  | 109    | 646    |
| 30    | OE_CTRL                | 109    | 397    |
| 31    | <i>Do Not Connect</i>  | 109    | 181    |

Note: for optimal Phase Noise performance, it is recommended to bond all optional VDD and GND pads.

